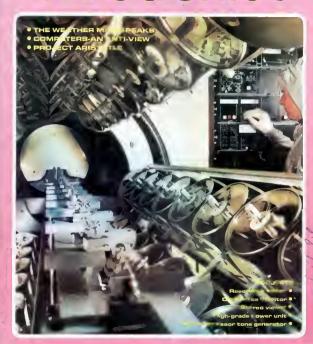
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CAN BRITAIN MAINTAIN ITS LEAD IN MOBILE RADIO?

One of the great success stories in the United Kingdom electronics industry over the past few years has been, and still is, mobile radio. Britain's world lead in this field has helped to push the number of two-way mobile radios in the UK to well over a million. Cellular radios, although they became available only in 1985, already account for over half that total. And demand keeps growing.

But while demand continues to grow, there are increasing shortages of skilled engineers and technicians to produce, install and service the equipment. According to the Federation of Communication Services (FeGs, the mobile radio market is growing at well over 10 per cent per year, while a survey of its members shows that 90 per cent of them need more technical staff. One industry source estimates that 6,000 more specialist staff will be needed by 1995.

There are several initiatives that mobile radio firms should make the most of to demonstrate that mobile radio offers excellent career prospects. These include the Enterprise and Education Initiative, which aims to strengthen the partnership between business and education by offering young persons the opportunity of gaining work experience in both manufacturing and service industries, and teachers the chance to experience business first hand. Another effective way of drawing school-leavers' attention to the radio industry is through the Young Radio Arnateur of the Year Award. This is aimed at anyone under 18 who is keen on Diy radioconstruction or operation, uses radio for a community service, or is involved in amateur radio in some other way, for instance, a school science project.

One of the main problems in mobile radio is the lack of nationally recognized qualifications for technicians. Trainees are often attracted to other sectors where structured training exists. The mobile radio industry itself faces difficulties when recruiting technicians of indeterminate abilities. Consequently, mobile radio users suffer because of the varying quality of service they receive.

These problems led the Department of Trade and Industry, the Mobile Radio Users Association (MRUA), the Federation of Communications Services and the Electronics Engineering Association (EEA) to Start the Radio communications Quality Assurance Scheme. For a company to maintain certification with the scheme, technicians must be properly trained and qualified. Recognizing this, the Dru and the MRUA earlier this year launched a joint initiative. This resulted in the Mobile Radio Training Committee (MRTC), whose aim is the identification of the mobile radio community's education and training needs.

The dialogue between academics and industry is important. Academics have expressed the view that business people should participate in planning courses and helping to provide on-the-job experience. Educators and trainers should be up-dated by working with businesses, having contact with senior engineers and experiencing the use of modem equipment.

The activities of the DTI, the MRUA, the FCS and the MRTC are drawing attention to the importance and growth of mobile radio. The United Kingdom currently has a leading role, but this position is threatened by the shortage of skilled personnel.

The Government is doing much to highlight the career opportunities and alleviate the problems, but the onus must be on business to form a partnership with education. Packages are required that will attract the people needed, in the numbers required, and provide them with the necessary skills.

Front cover

Clear compact discs prior to being metallized are seen during production at Numbus Records Ltd, Britain's largest manufacturer, whose development of a new laser-mastering system won the Queen's Award for Technological Achievement in 1987.

Producing a CD master with the Nimbus lasermastering system involves transferring up to 6,000 million bits of information (recorded sound) on to a prepared glass master. This is then transferred to metal stampers by an electro-forming process. The discs are pressed from clear polycarbonate by fully automated injection moulding presses.

A HIGH-GRADE POWER UNIT

C. Bolton BSc

These supplies were developed to power experimental electronic equipment including small RF oscillators and amplifiers. There are two versions: a single-channel unit and a dual-channel unit in which the channels may be used independently or in series to give well-balanced positive and negative rails.

Various circuits may be used to produce a variable, regulated output voltage:

Chopper circuits

In these, the current is chopped into pulses which are fed to an energy storage device to give an output voltage. This type of circuit was discounted for the present design since the switching involved produces RF energy which readily interferes with other equipment.

Shunt regulators

These circuits produce a larger current than is required, and shut the unwanted part away. The shunt regulator is particularly wasteful when the required current is much smaller than the available current, as is frequently the case in experimental work.

Series regulators

These are in essence series resistors that can be varied to maintain a constant output voltage. Their inefficiency is highest High-grade power supply Measured performance of each channel: 0-25 V fully variable Output voltage: Output current: 1.5 A max Current limit: 50 mA-1,5 A Output resistance: $2 m\Omega$ Output change for 10% mains change: <1 mV Total ripple plus noise <1 mV Dual-channel unit only:

at low output voltage settings and high load currents. Since the ability to power such a load was considered to be the least

Output balance: within 10 mV, retained

under current limit conditions

frequent requirement, this type of circuit was chosen for the design.

The measured performance of the units is summarized in Table 1.

Single-channel unit

The circuit diagram of the single-channel power unit is given in Fig. 1. The output current is produced by Tr. Br1 and Cr. The output working je is controlled by a series regulator in which Tr. Tr. and Tr. are the active elements. In effect, these transistors for an anulti-stage emitter follower that is driven by oppany ICr. The current gain and the use of Darlington-type power transistors for Tr. and Tr. ensure a small current demand on ICr. Transistors Tr. and Tr. are connected in parallel with small emitter resistors to distribute heat dissipation.

The output voltage of IC: is determined initially by a reference voltage applled to its non-inverting input. The

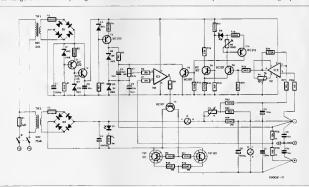
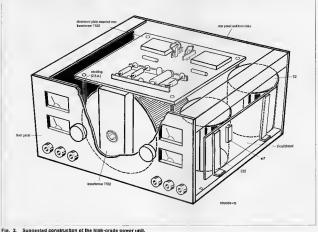


Fig. 1. Circuit diagram of the single-channel version of the power supply.



rig. 2. Suggested construction of the high-grade power unit.

Inverting input is a fixed fraction of the output voltage supplied by the unit. The high gain and differential operation of ICI enable the device to vary its output voltage such that the voltage difference between its inputs is almost zero.

The reference voltage for IC1 is derived from constant-current source Ts and sener diode Ds. Components Rs and Cs. form a simple noise filter. Zener diode Ds produces a small off-set voltage to enable the output voltage to go down to zero.

Current limiting on the basis of voltage feedback is achieved by R19, IC2, T9, T10 and To. The current flow through Rio produces a voltage across the resistor. Part of this voltage is selected by potential divider P2 and R20, amplified by IC2 and applied to a trigger circuit around Ts and To. Normaily To is off, but it is turned on when the output of IC2 rises sufficiently because of a higher load current. This causes LED Do to light, indicating current limiting activity, and Tis to be switched on. Transistors To, Tin and To now act as an amplifier to draw current through Rs, which in turn reduces the reference voltage to IC1 and, consequently, the output voltage.

Power to operate the reference source and associated circuitry is obtained independently of the output supply from Tr₁, Br₁ and C₁, together with stabilizing circuit T₁ and T₂. Loading on this supply is constant until current limiting occurs. The regulator for this supply thus acts only against fluctuations on the mains, which rarely reach 10%. This enables a steady reference to be obtained fairly simply.

Practical points

Component layout is not critical, but altention must be paid to a number of points. The can of C2 must be well sleeved to keep it insulated from the chassis. The wires carrying the output voltage must be routed such that fley do not form loops enclosing other components (this is most likely to happen on the from I pands). On a likely to happen on the from I pands). On a current must be thick enough to prevent under heating, and the wire connections at the output terminals must be made exactly as shown in the circuit diagram.

As to cooling, T4 and T7 must be mounted on a heat-sink with a thermal specification not exceeding 0.5 K/W. Remember to insulate these transistors electrically from the heat-sink. Transistor T2 requires only a small heat-sink.

Fuses Fr and Fr are intended to protect the rectifier bridges and the transformers against failure of the smoothing capacitor. They consist of short lengths of 40 SWG copper wire. Fr between vero-pins on the circuit board, and Fr between tags on a short length of tag strip, which can be mounted anywhere convenient to the transformer leads.

Any type of non-steel cabinet may be used to house the power supply. Steel may be used provided the main transformer has sufficiently small magnetic leakage to avoid magnetizing the steel near the leads to the inputs of ICs.

Constructional details of a cabinet that may be made from aluminium are given in Fig. 2. No dimensions are given since these will depend on the components used for Tr., Cr and the heat-sink. The L-section is extruded aluminium, which is available from many DIY suppliers.

Setting up

The setting up procedure is concerned entirely with the current limit facility.

 With the unit switched off, set the output voltage control, P₁, for zero volts, the current limit control, P₂, for maximum current (maximum resistance), and P₃ to zero resistance.

Connect a resistor of about 10 Ω, capable of carrying 1.5 A, across the output terminals (a length of electric fire spiral has been found useful).

nas been round usemi).

3. Switch on the unit and raise the output until a current of 1.5 A flows.

4. Adjust P so that the current limit warn-

ing light, D6, is just on.
5. Increase the resistance of P3 until the

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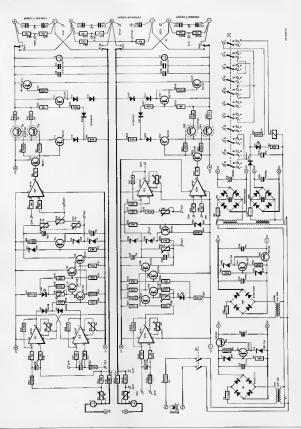


Fig. 3. Circuit diagram of the dual-channel PSU-10-20 alektoryndus october 1969

current drops by between 50 and 100 mA as indicated on an ammeter.

6. Reduce the output voltage to zero and check that the warning light goes out. Raise the output voltage and check that the warning lamp comes on at 1.5 A.

8. Try to raise the current by raising the output voltage or reducing the load resistor, and check that there is little rise in output current. 9. Choose other settings of the current

limit control, and check that limiting occurs at lower currents The lower limit should be between 30 and 50 mA.

10. If at any time the current limit indicator lights, but at less than full brightness, the limit circuit oscillates because Ps has been advanced too far and should be readjusted. This is best done by reducing its value to zero and repeating operations 3, 4 and 5.

The current limit control can be calibrated by setting it to maximum, adjusting the output current to a value required as a calibration point, and then adjusting the limit control until limiting just occurs as indicated by the lamp coming on.

Nates an the use

The output of the single-channel unit is floating so that either side, or none, may be grounded. The high degree of regulation is available only direct at the output terminals of the supply: bear in mind that six inches of ordinary connecting wire have a higher resistance than the output resistance of the unit. Under near short-circuit conditions,

the current limit may produce a low-level oscillation on the output voltage. This is dependent on the reactance of the load, and is unlikely to be of any consequence since the supply is not normally used as a constant-current source.

Dual-channel unit

In the dual-channel unit, channel 1 is essentially the same as the single-channel unit. The modifications are the addition of a fine voltage control, Ps, a second current limit amplifier, IC1, which is operational only in the balanced mode, and a discharge circuit, T11, T12 and T13, which discharges Co when the voltage setting is reduced, enabling the output to follow the setting closely. Channel 2 is similar to channel 1 except



Fig. 4. Auxiliary circuit for adjusting the

that it is complementary. For ease of following, the circuit components with an identical function in channel 1 and the single-channel version are given the same reference numbers. Likewise, components in channel 2 serving the same function as those in channel 1 are given the same numbers with prefix '9'. Thus, IC1 of channel 1 becomes IC91 of channel 2. The complete circuit diagram of the dualchannel power supply is given in Fig. 3.

The discharge circuit

As the voltage setting is reduced, the output of IC1 falls, and will fall below the output terminal voltage unless Cs is discharged The output voltage of IC1 is developed across R33 via emitter followers T5 and T11. Diode D10 produces a small voltage to compensate for additional baseemitter drop in Darlington transistors T4 and Tr. If the voltage across R13 is lower than that across Co., T12 is turned on. This in turn switches T13 on, which discharges Co until the voltage across it is almost equal to that across R33 when T12 is turned off. Components D12, D13 and R36 limit the base current in T13 to a safe level. Diode D11 prevents the base of T12 being driven dangerously positive if the voltage setting is raised suddenly.

Balanced autput made

In the balanced output mode, the operation of channel 1 is unchanged. In channel 2, the reference voltage is obtained from the channel 1 reference via the 'times-1' amplifier, IC4. This reference is compared with 34 of the voltage between the positive and negative rails produced by potential divider R39-R41

If the current in channel 1 exceeds the set limit, IC2 causes the limit circuit to operate. If the current in channel 2 exceeds the limit setting, the output from IC3 causes the limiter in channel 1 to operate. Since both channels use the channel 1 reference, they are limited equally in both cases. Hence, balance is maintained under current limiting conditions. Diodes Da and D+ prevent competition for limiting between the channels. The current limit settings of the two channels are independent Switching between modes of operation

is accomplished by S2, which is a wafer switch made up of two 6-pole, 2-way wafers. Relay Rei is operated by Si to switch the output current

Current for the relay coil is obtained from the channel 2 AC supply via Di4 and C15. This supply also feeds D7, the 'power-

on' indicator.

Setting up pracedure With the unit set for independent channel

operation, set the current limit circuits as described for the single-channel unit. Use Pa and P4 for channel 1, and P93 and P94 for

To adjust the balance, either a digital

voltmeter capable of resolving millivolts at 25 V and below, or the auxiliary test circuit shown in Fig. 4, is required. The PSU must be switched on at least five minutes before the balance is adjusted.

Turn S2 to balanced operation. Set channel 1 to about 10 V and adjust P7 so that channel 2, now the negative rail, also supplies 10 V.

Setting up with a DVM 11. Set the output voltage to about 19 V

with the aid of the channel I control 12. Connect the digital meter to the + and ± terminals. Note the reading

13. Connect the digital meter to the ± and - terminals, Adjust P7 to give the reading obtained in step 12 14. Reconnect the digital meter to the +

and ± terminals. Reduce the output voltage to 1.5 V and note the exact reading 15. Connect the digital meter to the ± and - terminals. Adjust Ps to give the reading obtained in step 14

Setting up with the auxiliary test circuit 11. With the 18 V battery in the test circuit and the multimeter on the 25 V range, connect point X to the + terminal, and point Y to the ± terminal. Adjust the output voltage so that the multimeter reads zero. Change to 100 mV and adjust the output voltage to give a multimeter reading of

Set the multimeter to the 5 V range. Connect X to the ± terminal, and Y to the - terminal. Adjust Pr until the multimeter reads zero. Change the multimeter range to 100 mV and adjust P7 to give a reading of 50 mV. 13. Disconnect the test circuit from the

unit. Replace the 18 V battery by the 1.5 V cell in the test circuit. Reduce the output to about 2 V and set the multimeter to the 5 V range. Connect X to the + terminal, and Y to the ± terminal. Adjust the unit until the multimeter reads zero. Change the multimeter range to 100 mV and adjust the output voltage to give a reading of 50 mV.

14. Set the multimeter to the 5 V range. Connect X to the ± terminal, and Y to the terminal. Adjust Ps so that the multimeter reads zero. Change the multimeter range to 100 mV and adjust Ps to give a reading of 50 mV.

Further settings common to both methods: 16. Repeat steps 11 to 15.

17. Repeat steps 11, 12 and 13 If any adjustment of P7 is required, steps 14 and 15 must be repeated, followed by steps 11, 12, and 13 and so on until no further adiustment is required.

 Connect the 10 Ω resistor used for setting the current limit to the ± and - terminals. Set the channel 2 current limit control for maximum current, and adjust Pe so that the channel I limit warning lamp just comes on when the current in channel 2 (the negative rail) reaches 1.5 A

COMMUNICATION RECEIVER FRONT-END FILTERING

by A. B. Bradshaw

In communication receivers, whether intended for general coverage or for amateur bands only, front-end design has changed considerably over the years. With the use of higher intermediate frequencies (e) and the availability of high-frequency (ive) crystal filters, we no longer see the multiple banks of funed circuits and multigang capacitors.

Unfortunately, for most new developments there is a price to pay, the reduction in pre-mixer selectivity means that any amplifier preceding the mixer must offer superlative performance in terms of intermodulation distortion and cross modulation. If it does not, the user may get the impression that the receiver is full of signals. The old saying that "The wideer the window's open, the more muck blows in" is very upt here. It was with these thoughts in mind that

It was with these thoughts in mind that the writer has designed some general-purpose Front-end filters for the amateur hands. If you need more protection up front when Joe Bloggs just down the road fires up his 400 watto of sideband, these filters should help you to listen on the next adjacent band up or down. You may wish to incorporate them in your next receiver.

What kind of filter?

Frequency filters fall into four categories: low-pass (LP), high-pass (HP), band-pass (BP), and band-stop. The design of a band-pass filter for rel-

atively small bandwidths is not too difficult, but the difficulty increases exponentially with increasing bandwidth!

Band-pass and band-stop filters may be constructed from a mix of low-pass and high-pass actions. In Br filters, these secitors are in sense on band-stop filters they are in parallel. The band-stop filter so constructed is not often seen in print, but in nevertheless, a thoroughly practical design. It is, of course, a pity that the LP and his sections can be used only for the construction of a band-pass or a band-stop filter, but not for both simultaneously!

In modern filter design, a number of approximations to the ideal brickwall response have become popular. The low-pass responses of these are shown in Fig. 1. Their high-pass response is obtained by network transformation.

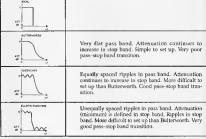


Fig. 1. Frequency response characteristics of the ideal low-pass lilter and three approximations.

The operating impedance, band edge, attenuation in the stop band, pass-band ripple and component values are all derived from a low-pass section normalized for a frequency of I radian and an impedance of I Ω .

The shape of the response, which determines the complexity (tength) of the finished filter, is decided with the aid of design tables. There is usually a trade-off between the ratio of the band-edge frequency to the design attenuation frequency and the stop-band attenuation. This means that the 'squarer' the response of a given filter is, the lower will be the stop-band attenuation.

In the construction of a BP filter, the band edge of the LP section becomes the upper profile and that of the HP section, the lower profile. In effect, the two responses cross over each other. In the designs illustrated in this article,

the elliptic function approximation is used. With this, the minimum stop band attenuation remains at its design figure, in contrast to Butterworth or Chebishev functions where it increases the turther the frequency is away from the band edge. This is, however, a small price to pay for the excellent transition band selectivity of this type of filter.

The filters discussed here are designed

for a stop-band attenuation of 40 dB or 80 dB to meet both light and stringent requirements. Also, they are designed for an input and output impedance of 50 Ω. Although intended primarily for receiver applications, they may, of course, be used in transmitters, in which case the component ratings MUST BE UPGRADED!

Components

Ideally, the filters should be constructed on a printed-circuit board, but this is not essential

Capacitors should be low-loss types. They should be connected in parallel to get their tolerance within 1%, although silver-mica capacitors with 1% tolerance are readily available.

The Q of the inductors should be as high as can be obtained. However, as the filter impedance is $50~\Omega$, the values of inductance are low, so the coils can be wound manually quite easily. Take care to prevent inductive coupling between sections.

When setting up the filter, trim the coils to their correct value by checking the stop-band nulls on an oscilloscope (or analyser if you are that lucky!). Check all frequencies with a suitable counter.

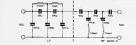


Fig. 2. Band-pass filter for the top band. The -1 dB edges are at 1.8 MHz and 2.0 MHz. The pass band ripple is 1 dB. The -40 dB points are at 1.479 MHz is 0.18 dB. The pass band ripple is 0.18 dB. The -80 dB points are at and 2.434 MHz. The frequencies of infinite attenuation are at: LF 1.025 MHz 3.178 MHz and 1.132 MHz. The frequencies of infinite attenuation are at: LF and 1.44 MHz; HF 2.5 MHz and 3.51 MHz.

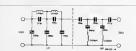


Fig. 4. Band-pass fifter for the 80 m band. The -1 dB edges are at 3.5 MHz Fig. 5. Band-pass fifter for the 80 m band. Attenuation at 3.5 MHz and 3.8 and 3.8 MHz. The pass band ripple is 1 dB. The -40 dB points are at MHz is 0,18 dB. Pass band ripple is 0.18 dB. The -80 dB points are at 2875 MHz and 4.624 MHz. The frequencies of infinite attenuation are at: LF 2.202 MHz and 6.038 MHz. The frequencies of infinite attenuation are st: LF 2.8 MHz and 1.994 MHz: HF 4.75 MHz and 6.669 MHz.

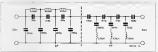
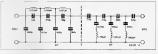
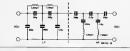


Fig. 3. Band-pass filter for the top band. Attenuation at 1.8 MHz and 2.0 0.9269 MHz. 1.1106 MHz and 0.54202 MHz; HF 3.88 MHz, 3.241 MHz and 6 641 MHz



1.053 MHz, 1.802 MHz and 2.159 MHz; HF 6.158 MHz, 7.378 MHz and 12.619 MHz.



and 7.2 MHz. The pass band ripple is 1 dB. The -40 dB points are at 5.751 MHz and 8.762 MHz. The frequencies of Infinite attenuation are at: LF 3.988 MHz and 5.6 MHz: HF 9.0 MHz and 12.63 MHz.

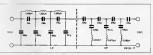


Fig. 6. Band-pass filter for the 40 m band. The -1 dB edges are at 7.0 MHz Fig. 7. Band-pass filter for the 40 m band. Attenuetion at 7.0 MHz and 7.2 MHz is 0.18 dB. The pass bend ripple is 0.18 dB. The -80 dB points are at 4.405 MHz and 11.44 MHz. The frequencies of infinite attenuation are at: LF 2.107 MHz, 3.604 MHz and 4.319 MHz; HF 11.668 MHz, 13.981 MHz and 23,91



Fig. 8. Band-pass filter for the 20 m band. The -1 dB edges are at 14.0 MHz and 14.2 MHz. The pass band ripple is 1 dB. The -40 dB points are at 11.50 MHz and 17.28 MHz. The frequencies of infinite attenuation are at: LF 7.977 MHz and 11.2 MHz; HF 17.75 MHz and 24.92 MHz.



Fig. 9. Band-pass filter for the 20 m band. Attenuetion at 14.0 MHz and 14.2 MHz is 0.18 dB. The pass band ripple is 0.18 dB. The -80 dB points are at 8.810 MHz and 22.564 MHz. The frequencies of infinite attenuation are at: LF 4.215 MHz, 7.209 MHz and 8.638 MHz; HF 23.01 MHz, 27.57 MHz and 47.156 MHz.



Fig. 10. Band-pass filter for the 10 m band. The -1 dB edges are at 28 MHz and 30 MHz. The pass band ripple is 1 dB. The -40 dB points are at 23 MHz and 36.51 MHz. The frequencies of infinite attenuation are at: LF 15.954 MHz and 22.4 MHz; HF 37.5 MHz and 52.65 MHz.



Fig. 11. Bandpass filter for the 10 m band. Attenuation at 28 MHz and 30 MHz is 0.18 dB. The pass band ripple is 0.18 dB. The -80 dB points are at 17.62 MHz end 47.6 MHz. The frequencies of infinite affenuation are: LF 8.43 MHz, 14.419 MHz and 17.277 MHz; HF 48.619 MHz, 58.254 MHz and 99.625 MHz.

AMATEUR COMMUNICATION RECEIVERS: STILL A CHALLENGE?

by A. B. Bradshaw

The valve ero

Over the past forty years or so, communication receiver design has undergone quite a revolution. In the days before transistors and ics, there were some remarkably good receivers around. Typical among these were the ARS8, the Hamerlund Super-Pro, the Marconi CR 100, the BCG348, and the Racal RA17. After the end of the Second World War,

many radio amateurs were using either one of these classical designs or one of the many ex-military receivers that had come on to the surplus market.

A large number of amateurs showed great ingenuity in the use of various liems of military equipment to make up their staminter as well. There was a lot of ex-services expertise about and a considerable amount of technical discussion seemed to take place over the airwaves. Cobbin together all this readily obtainable gear was not entirely caused by the non-availability of proprietury amateur equipment most of us being broke had something to do with it as well.

Towards the end of the valve era, there occurred a number of technical developments in radio valve technology that had a direct bearing on communication receiver design. One of these was the appearance of the frame grid pentode, like the E183.

These new valves, 465 kHz IF transformers with a good Q, and ex-government quartz crystals, such as the FT241/243, helped to achieve respectable IF response shapes for reception of the increasingly popular single-sideband (ssb) transmissions.

At the same time, wide-range, stable automatic gain control (AGC) was becoming the norm, its control voltage no longer derived from the incoming carrier.

The emergence of the long-life stable double triodes, like the E88CC, originally developed for the then embryonic computer industry, further helped to improve amateur communication receiver design.

Another milestone was the introduction of the beam deflection mixer valve, like the 6AR8 and the 7360, which were developed for the American colour TV market. The remarkably linear mixing and large-

signal handling capabilities of these new valves soon caught the eye of receiver designers and it did not take long before manufacturers like Collins, Squires-Sanders, Drake, and so on were incorporating them in their new receivers.

At about this time, a superb receiver, the Thombey GDDAF design, appeared on the UK amateur scene. Many of these excellent receivers were built and had a profound influence on our thinking of what kind of performance could be achieved with the technology then available. I built my own and well remember the pleasure of using the receiver, which had the knife-edge selectivity of the Kokusai mechanical filter Type MF455-10.K.

By then, we had the ingredients necessary for meeting the specification for a good communication receiver:

 good tF shape factor (in spite of the low iF resulting from the multi-conversion necessary for the HF end);

 stable conversion oscillators, necessary for the increasingly popular SSB mode of transmission;

 ease of tuning with mechanical s/M drives (Eddystone 898, and so on).

Nevenheless, these receivers still had some serious short-comings. They were complex (at the time); they assually mebodied lots of ganged switching of tuned circuits; they used relatively expensive wound components; their front-end alignment and tracking, particularly in general coverage designs, was difficult; and lastly, these 'magificent machines' could certainly not be regarded as portable.

The solid-state ero

The transition to solid state electronics was not a sudden occurrence, and for some years hybrid designs were very popular in the amateur press. Although these designs still used valves in their frontends, much of the remaining circuitry had become solid-state. These early solid-state devices, however, could not produce the good intermodulation and cross modulation performance of their valved predecessors.

Over the past decade, solid-state

devices have improved enormously, however, and present-day communication receivers have very real benefits compared with those of yesteryear.

Unfortunately, in my view, we have allowed the Japanese industry to dominate the manufacture and design of good quality communication receivers. This is particularly disappointing in view of our own earlier performance. In the solid-state erawe have managed to produce some innovative designs, but they are few and far between.

Nevertheless, the radio amateur remains in a unique position. The receiver manufacturer is hamstrung by severe economic restraints and market forces. The amateur designer and constructor, on the other hand, is still at liberty to explore and indulge his fancy in ways that would be out of the question for the professional designer. I am not suggesting for one moment that the radio amateur can challenge the Japanese glants. Nevertheless, there is still much innovation in Britain, well documented in a variety of books, technical articles, application notes, and so on.

Modern home construction If we regard the modern communication

receiver at a system level, we have a good opportunity to see what some British manufacturers and suppliers have on offer RF amplifiers: Plessey Types SL600; SL611C; SL612; SL1610C; SL1611C; SL1610C; SL611C; SL612; SL610C; SL611C; SL610C; SL610C; SL611C; SL610C; SL610C;

High performance mixers: Plessey Type SL6440/AC (430 dBm intercept point): Siliconix Type S18901 double-balanced mixer (435 dBm intercept point); various diode bridge ring devlees, from the MD108 up to the SRA3 (£28 from Cirkii), ir shaping filters ceramic and mechanical filters are available for the lower treare quartz crystal lattices up to 10.7 MHz, are available in bandwidths suitable for AM, \$88 and Cw from Cirkit. Ir amplifers: three Plessey Type SL612

ICS will give most of the gain required in a normal if amplifier.

Demodulators for AM, SSB, and CW; Plessey Types SL6700A and SL624. AGC generators: rather a limited choice here, but the Plessey SL620 and SL621C tCs are well proven.

This list shows that there is a good home-bred range of building blocks, although I still feel that there are areas of design that have been neglected. Some of these are receiver front-end filtering for the anateur bands, local oscillator design (either upper conversion synthesis or limited-range 870 conversion systems), while the required noise floor specification for vite synthesizers is a real challenge.

Conclusion

As I glance through yesteryear's copies of RSGB Bulletin, RAD COM, and others, I can not but be struck by the falling off in Interest in innovative design. Can this malaise be halted? I certainly hope so. What are you going to do about it?

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1980 (in 6 parts),
"The RX80 Mk2" by A.L. Bailey, Rad
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NEW PRODUCTS

Thick Film Resistor Arroys (DIP)

Honest (YEC) Inc., Japan, offers Dipped Resistor Networks Dual in Line Package (DIP). As these are dipped components, they are cheaper when compared to moulded ones. Circuits are available in Isolated, Bussed and Dual Terminators. These arrays have a pitch of 2.54 mm and hence compatible with standard I.C. sockets, Power ratings offered are 0.063 W, 0.125 W and 0.25 W. Resistance tolerances offered are +20%, +10%, +5% +2% . Resistance range is from 50 ohms to 1 M ohm. T.C.R. available are 300, 250 and 200 ppm/C. Operating temperature range is from .55 C to +125 C.



Hi-Tech Resistors Pvt. Ltd. • 1003/4, Maker Chambers V, Nariman Point • Bombay-400 021 •

Contoct Cleoner

ACCRA PAC (INDIA) PRIVATE LTD. in collaboration with Acera Pac Inc., USA, have introduced the SAFEGUARD Contact Cleaner, for electronic maintenance.

The Contact Cleaner is a specially formulated solvent which restores electrical continuity of all types of contacts and controls. Pure solvents under high pressure quickly penetrate the surface pores removing grease, dirt, oil and surface oxides, and evaporate quickly leaving behind clean contacts. It has excellent dielectric properties and improves performance and reliability of all electronic equipment. Non-flammable, non-toxic the Cleaner is useful for silver/precious metal contacts, TV turners, miniature controls, solenoids, circuit breakers, potentiometers, selector switches, volume and tone controls, relay contacts, thermostat controls, distribution panels and other electronic/electrical contacts.

ACCRA PAC (INDIA) PRIVATE ETD ● 917, Raheja Chambers ● Nariman Point ● Bombay-400 021 ●

Vinyl Hoses

Udey Cables are manufacturing Parmyficx Flexible Vinyl House for various applications like electrical conduits in buildings, machine tool wrings, dust and rags collection hoses for textile machinery, Vacuum cleaner hoses, gas and fume removal, dust extractor for wood wrking etc. Reinforced with steel wire to ensure resistance to crushing forces and development of kinks the hoses are available in diameter 10 to 60 mm for medium duty application (Type SF) and medium duty application (Type MSF). Others a vailable against specific orders.





Udey Cables • C/o. Jafkay Lights • Dina Building • 52 M. Karve Road • Bomhay-400 002 • Tcl: 314622/310870 •

STEREO VIEWER

C.J. Ruissen & A.C. van Honwelingen

This electronic ornament is basically an unconventional VU-meter. A square matrix composed of 10×10 LEDs indicates signal volume as well as stereo information.

The circuit is perhaps best qualified as a simple X-Y display for audio signals, and the displayed patterns are, therefore, not unlike Lissajous figures. The heart of the circuit is formed by an integrated circuit from National Semiconductor, the Type LM3914. At first glance, this dot/bar display driver is a quite conventional design. The IC houses ten comparators, a precision linear-scale voltage divider and a reference voltage source. The actual realization of these parts, however, gives the LM3914 a number of interesting fea-

- outputs drive LEDs, LCDs, fluorescent displays or miniature bulbs
- · external input selects bar or dot display · simple to cascade for displays with a
- resolution of up to 100 steps internal voltage reference; adjustable be-
- tween 1.2 and 12 V minimum supply voltage: 3 V
- current-regulated open-collector out-
- output current programmable from 2 to
- no multiplex switching input withstands ±35 V
- · outputs interface direct with TTL and
- CMOS logic · floating 10-step divider can be connected
- to a wide range of voltages, including internal reference

Circuit description

The circuit diagram of the 10×10 LED matrix which determines the appearance of the stereo viewer is given in Fig. 2. The dimensions of the matrix result in a square arrangement How the square is actually positioned is a matter of personal preference, and not, of course, of any circuit configuration. The introductory photograph shows the prototype which has matrix co-ordinate X1-Y1 below and X10-Y10 at the top.

The matrix arrangement allows any one of the 100 LEDs to be turned on and off individually. To select a particular LED, the relevant column, X1-X10, and row, Y1-Y10, is made high and low respectively. The circuit diagram of the row/column driver (Fig. 1) shows that two LM3914s are used: IC2 forms the column driver (X-axis), and IC3 the row driver (Y-axis). Both LM3914s are set to



operate in the dot mode so that, strictly speaking, one row and one column are selected to light one LED at a time. The IC outputs have some overlap, however, so that two LEDs are on at the switch-over

Transistors T2-T11 function as inverters. They are required because the column driver must switch to the positive supply rather than to ground. The programmable current source in 1C3 is set to supply the relatively small base currents for the inverter transistors. The current source in 1C2 is set to a much higher value to supply the required current direct to the LEDs

The current source in the LM3914 is set in a rather unconventional manner: the output current is ten times the current supplied by the reference voltage. So, all that is required is to load the reference of ICs to about 2 mA. A slightly different approach is used in the case of ICz here, an LDR (light-dependent resistor), a transistor, Ti, and a handful of other components form a load resistor whose value is a function of ambient light intensity. Since the output current of IC2 is used for driving the LEDs, the display intensity is automatically controlled as a function of ambient light conditions. The component values used allow the LED current to vary between 8 and 25 mA. To make sure the LEDs are completely

off when they have to be off, the LI outputs of IC2 and IC3 are fitted with a pullup resistor. This is required because the I.1 output has an auxiliary current source that is used for cascading driver chips to form a larger display. The pull-up resistors keep T2 from conducting, and one

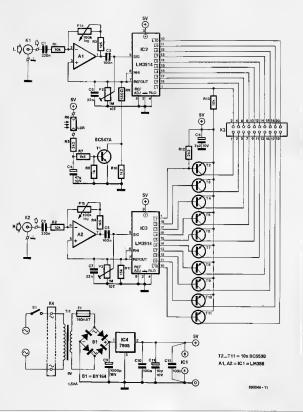


Fig. 1. Circuit diagram of the stereo viewer.

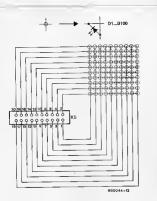


Fig. 2. Matrix configuration with 100 LEDs.

LED in the matrix from lighting, when the LT output is not actuated

The audio signals applied to the stereo viewer are first attenuated to enable the drive levels for ICs and ICs to be set accurately. The sensitivity of the circuit is set with potentiometer Pt. Acceptable drive levels at the inputs are between 45 mV and 3 V.

The zero point of the matrix is shifted to the centre of the square display with the aid of blas voltages on to which the AF signals are superimposed. These voltages are obtained with multiturn presets P₂ and P₃, which are adjusted to supply half the reference voltage. A voltmeter is not required for this adjustment, because the zero indication can be seen to shift to the

Parts list

Resistors (±5%): R1;R2;R13 = 10k R3;R4 = 1k5

Rs;R12 = 2k2 Rs = LDR R7 = 1k8

R₁₀ = 560Ω R₁₀ = 1k2

R₁₁ = 15k P₁ = 100k logarithmic potentiometer;

P2;P3 = 1MΩ multitum preset

Capacitors:

C1;C2 = 220n C3;C5;C10;C12 = 100n C4 = 47µ; 10 V C4;C7 = 22n C6 = 2µ2; 10 V

Ce = 2μ2; 10 V Ce = 1000μ; 16 V; radial Ctt = 10μ; 10 V

Semiconductors: B1 = BY164

D1-D100 = LED; dia. 5 mm T1 = BC547A T2-T11 = BC559B

IC1 = LM358 IC2;IC3 = LM3914 IC4 = 7805

Miscellaneous:

F1 = 160 mA tuse with PCB mount holder. S1 = SPST mains switch. Tr1 = PCB-mount transformer 9 V; 1.5 A.

K₁;K₂ = phono socket. K₃ = pin header 2×10 contacts.

K4 = 2-way PCB terminal block. K5 = IDC header 2×10 contacts.

PCB Type 890044

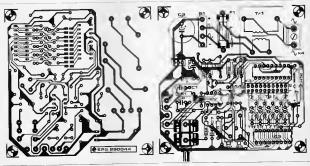


Fig. 3. Track layout and component mounting plan. 10.28 elektor indus actober 1989

centre of the display.

The circuit is powered by a conventional regulated 5 V supply, which is fitted on to the printed-circuit board together with the associated mains transformer.

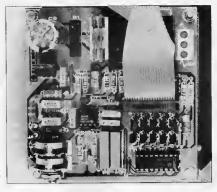
Construction: simple

The printed-circuit board shown in Fig. 3 accommodates all parts except the LED matrix and the LDR for the display intensity control. Populating the PCB is entirely straightforward if the wire links are installed first.

The LED matrix is built separately on

a square piece of veroboard. The installation of the LEDs and the lozenge shaped wring at the rear of this board are greatly simplified when the matrix is turned 45° with respect to the hole pattern in the board. The LED matrix is connected via a short length of flat-ribbon cable, for which a mating 20-way pin header, K3, is provided on the main board.

The stereo viewer is simple to align: simply adjust P₂ and P₃ until the centre four LEDs in the matrix are on. The sensitivity can then be set as required with the aid of the volume control, P₁.



NEW PRODUCTS

Digital Multimeter

PLA has developed the DM-20A a digital multimeter.

Hawing an LCD display with a resolution of 1 ouV on 200 mV range in both AC? DC models. It has an accuracy of 0.1%. Maximum voltage measurable in DC ranges is 1000 V and 700 V rms in AC range. It has a resolution of 10 nA on 200 uA range in AC mode. It has wide frequency range of 20 KHz in AC voltage and is battery operated.

Applications are in R & D labs and colleges for calibration and measuring parameters. PLA ELECTRO APPLIANCES PVT. LTD. • Thakor Estate • Kurla Kirol Road • Vidyavihar (W) • Bombay-400 086 • Tel: 5132667/5132668/5133048 •

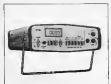
Photoeiectric Fork Switch

Electronic Switches, have developed Photoelectric Fork Switch also knows as Slot Sensor or Grooved Head Sensor. This is one piece device containing infrared light emitting diode, photo transistor receiver an amphifier. A solid state construction give it a long maintenance free life. Requires 10-24 Volts DC supply is protected from reverse polarity connecting the proceeding the process of the p

transperant foils, Edge alignment, space detection on toothed wheels, position sensing, for machine tools controls, other processing machinery etc.

Electronic Switches (Nasik) P. Ltd. •

1, Nahush • Gangapur Road •
Nasik-422 005 • Tel: 0253-78452





PC AS TONE GENERATOR

J. Schäfer DL7PE

A GW-BASIC program and a few modifications to the loudspeaker circuit enable any PC, whether an XT, AT or compatible, to function as a precision tone generator with a frequency range of 20 Hz to 120 kHz, with a basic sweep function as a useful option. The nice thing about this generator is that it costs next to nothing, while doubling as a frequency meter.

The present PC tone generator, which is really a BASIC program only, is ideal for aligning a wide range of AF circuits. The frequency of the generated tone can be set accurately, so that the low-cost tone generator is suitable for applications that include the tuning of musical instruments (electronic tuning fork), the aligning of RTTY, fax and SSTV filters, and the dimensioning and testing of many other types of tone decoder. In many cases, the BASIC program obviates the use of a function generator and a frequency meter. This is of particular interest for applications in the audio range, where frequency meters are, in general, not very accurate. The PC tone generator allows AF frequencies to be defined with an accuracy of a fraction of a hertz.

ated by the equipment under test can be read from the PC screen. Similarly, the PC tone generator can be set to a particular frequency, so that the oscillator can be adjusted until zero-beat is achieved.

If the generated tone is required electrically also, the loudspeaker signal must be made available on a jack socket — see Fig 1. When a plug is inserted, the loudspeaker in the PC is automatically dis-

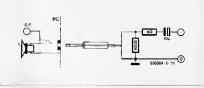


Fig. 1. Coupling out the PC's AF signel via a jack accept with a break contact.

PC as tone generator

Apart from the possibilities offered by BASIC commands #EF and SOLNO, there exists a more powerful way of generating tones with the aid of a personal computer direct control of the relevant hardware. This enables frequencies to be generated at quartz-crysial stability in the range from 20 Hz to several hundred kHz, independently of the PC's clock frequency. The lower frequency limit is rived, but the upper limit can be made as high according to the control of the con

ing.
The frequency resolution is excellent, especially in the audible range: at a basic frequency of 10 kHz, the step size is as small as 85 Ly. or 0.85%; between 2 and 3 kHz, the step size is 5 Hz (0.16%); and below 1 kHz, its 0.2 Hz (0.01%).

The PC generates the required tone via the bull-in loudspeaker. This is adequate for nearly all calibration and adjustment work in the acoustic range. An oscillator, for instance, is simple to calibrate accurately by means of a beat-frequency measurement in which the PC functions as the reference. Just compare the two tones by listening to them simultaneously, and step the PC tone frequency until the difference frequency decreases. When it becomes inaudible, the frequency energy

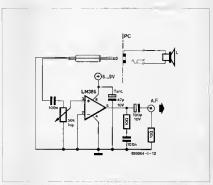


Fig. 2. The 'active' alternative: raising the PC's AF signal with the aid of a small amplifier.

abled, and the generated lone is available at a relatively low impedance. The 8 Ω resistor protects the internal AF amplifier against short-circuits. The value of this resistor must be increased as required if the internal loudspeaker is a high-impedance type. It is, of course, also possible to write the socket such that the loudspeaker is not disabled, but taken up in series with the output signal. This arrangement obsidence is a superior of the superior of the country of the connecting a 16 Ω resistor instead of the incitated 100 Ω type to ground, the generated tone is simultaneously audible via the internal loudspeaker.

A further possibility is shown in Fig. 2. A small amplifier with adjustable volume is connected to the jack socket. This solution is particularly useful for PCs that have an internal loudspeaker with a relatively high impedance, or one that produces insufficient output volume.

The program

The frequency range of 20 Hz to 120 kHz is fixed in lines 180 and 200 of the the BASiC program. Keys are used to control the program:

Key 'e': enable tone

Key 'd': disable tone Key '+': increase frequency by previously entered step size

Key '-': decrease frequency by previously entered step size

Key 's': terminate program

A frequency sweep is obtained by holding the + or - key — the tone frequency then increases or decreases at the previously entered step size.

Applications

Here are a few of the many possible applications of the computer-controlled tone generator:

- test signal for aligning RTTY circuits, e.g., 1275/2125 Hz for VHF stations, and
- 1275/1445 Hz for SW stations.

 test signal for tone decoders
- test signal for tone decoders
 1,000 Hz frequency reference
- tuning fork
- elementary acoustics

Table 1 is useful for the tuning fork application because it shows the tone frequencies for three octaves.

Table 1. Commonly used frequencies for tuning musical instruments.

```
10 REM PC Tome Generator
20 REM: by DL76E
30 CLS REY OFF
40 GOSUB 350
60 LOCATE 5,1
70 PRINT : PRINT : INPUT "
                                                                                                                             please enter start frequency : ",FREG
please enter step mize . ",STP
BO PRINT PRINT - INPUT "
90 (3.5
00 CLS
100 COMP 300
100 COMP 30
1/0 XS_INEVI $(1) IF XS= """ THEN FRRG= FRG0 + ST

100 IF FRED-120000' THEN FRED-120000! COSUB 250

100 IF MS= """ THEN FRED- FRED - STP

200 IF FRED-120 ITHEN FRED-20 - COSUB 250

210 IF XS= """ OR XS=""" THEN GOSUB 660

220 IF XS= """ ON XS=""" THEN GOSUB 660

220 IF XS= """ ON XS="" THEN GOSUB 660

230 IF XS= """ ON XS="" THEN GOSUB 660 COTO 250
 240 9070 125
 250 CLS : PRINT"
                                                                                          END
 260 REM : generate tone
200 REM : generate tone
270 Olf 67,182 - REM "load 182 from timer block "
280 LET COUNT-[193]#01/FRED.REM "compute dats for timer block"
290 LET CMTH-1NT (COUNT/256) REM "most-mignificant byte"
300 LET ONID-INT(COUNT = CNTH1*256) .REM "leset-mignificant byte"
 310 OUT 67,102
   320 OUT 66.CNTLO .REN "supply lesst-algoifIcent byte"
 330 OUT 66.CNTHI -REN "supply wost-significant byte"
   340 RETURN
 350 PRINT SPC(27):"TO NE GENERATOR '
355 PRINT SPC(33):"by DL7FE"
   360 PRINT"
   380 LOCATE 22,1
   390
 PRINT"
                                                              ":PRINT:PRINT "ksy functions :
 410 PRINT"
 420 COLOR 7,0
 440 COLOR 0.7
   450 PRINT" DOWN ":
 460 COLOR 7.0
470 PRINT "
 480 COLOR 0,7
 500 COLOR 7,0
510 PRINT "
   520 COLOR 0,7
   530 PRINT" OFF ":
   $40 COLOR 7.0
   550 PRINT "
 560 COLOR 0,7
570 PRINT" STOP ";
580 COLOR 7,0
610 LOCATE 5,26
                                          "range 20 Nz to : 100 kHz"
   620 ERINT
   630 RETURN
640 OUT 97, TNP(97) OR 3 .REM turn on PC loudspasker
 660 QUT 97, INP(97) AND 2S2 :REN turn off PC loudspeaker
670 RETURN
```

Note	4th octave	5th octsve	5th octave
C	261.6	523.3	1046.5
C#	277.2	554.4	1108 7
D	293.7	587.3	1174 7
D#	311.1	622.3	1244.5
E	329.6	659.3	1318.5
F	349.2	698.5	1396.9
F#	370.0	740.0	1480.0
G	392.0	784.0	1568 0
G#	415.3	830.6	1661.2
A	440.0	880.0	1760.0
A#	466.2	932.3	1864.7
н	493.9	987.8	1975.5

SIMPLE TRANSMISSION-LINE EXPERIMENTS

by Roy C. Whitehead, C.Eng., MIEE

This article describes some simple transmission-line experiments that were developed for the uncLE scheme. Under this scheme, which was initiated by the IEE, but later joined by other learned societies, members (usually retired) volunteer to go to schools to help teachers to bridge the gaps that exist between the academic world and the world of practical engineering.

The material used in the experiments consisted of:

- a known length of coaxial cable of which both ends were accessible;
- a twin-beam oscilloscope;
 an HF generator with 75 Ω output;
- three 100 Ω non-inductive notentiometers;

Meosurement of velocity rotio

The equipment should be connected as shown in Fig. 1. Set Pt to its maximum resistance value and the two Y sensitivity controls of the CRO to produce equal values of Y sensitivity.

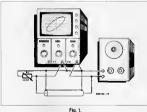
Set the signal generator to its minimum available frequency and note the small lateral displacement of the two waveforms. Then, increase the generator frequency, which causes the lateral displacement of the waveforms to mecrease, until, for the first time, the two waveforms are seen to be in phase. The propagation time of the cable now equals one period t = 1/9 of the generator output. The velocity ratio of the cable then equals

velocity in cable / velocity in free space =

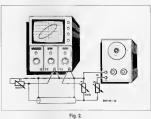
= cable length in metres ×f/(3×108).

A typical value is 0.8.

Change the generator frequency to one quarter of the value used previously, which makes the line one quarter wavelength long. Adjust Pt to obtain vertical Y deflections on the cro of equal magnitude.



rig. t.



Disconnect Pt and measure its effective value, which is equal to the characteristic impedance, Z_{co} of the cable.

Meosurement ot attenuation/ frequency chorocteristics

Connect the equipment as shown in Fig. 2. Set Rt to equal Z₀. Potentiometer Pt has been provided with a decibel scale (which can be done with the aid of the ohmmeter). Adjust R2 to provide across the input end of the line an impedance equal to Z_{or} If the output impedance of the generator is 75 Ω , this will be 43 Ω .

Over a range of frequencies, say from 100 kHz to the maximum at which the available equipment will operate satisfactorily, adjust Pt to produce Y deflections of equal magnitude. The cable attenuations are then equal to the attenuations of the potentiometer. The attenuation/frequency characteristic of the cable roughly follows the emperical equation

 $loss = (a\sqrt{f} + bf)$ [dB]

where b<<a so that the second

term becomes significant only at frequencies above about 16 MHz, owing to the skin effect. If a loss/frequency equalizer be designed and constructed, this

may be tested in a similar manner, after which the line plus the equalizer may be tested. Other tests may also be carried

out. For instance, short-circuit the output end of the cable at Y1 and note the effects on the Y2 waveform for odd and even numbers of quarter wavelengths. Repeat this test with an open circuit at

The relationships between cable length and the frequencies at which the CRO and generator can operate satisfactorily should be noted. The shorter the cable, the higher must be the operating frequencies of the generator and the CRO.

The connectors used should preferably be coaxial, otherwise they should be short, especially when operation is at frequencies above 10 MHz.

A NEW GENERATION OF ANALOGUE SWITCHES

by Jack Armijos and Tania Chur*

Most applications for analogue switches fall into two categories; signal routeing and signal conditioning. Different processing technologies produce switches with different characteristics. One advantage of the new CMOS analogue switches from Siliconix is that they allow you to control signals that fall anywhere between the two power supply rails. Furthermore, these

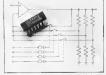


Fig. 1. The DG400 series of analogue switches.

high-performance silicon-gate tcs, the DG400 l'amily, are pin for pin replacements for the popular DG200 series. They offer significantly lower on-resistance $(r_{DS(OB)}=85 \Omega)$, lower power dissipation (35 μW), faster switching speed (ton= 250 ns) and lower leakage current (Is(off) <500 pA) than the older industry-standard parts. The new devices are shown here in typical circuits, illustrating the benefits they offer.

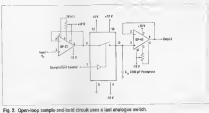
Sample-and-hald functions

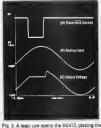
In most data acquisition systems, many channels are sampled sequentially and then digitized by an analogue-to-digital converter. In choosing or designing a sample-and-hold system, speed and accuracy are the two most important considerations.

Open-laop, cascadedfallower sample-and-hald circuit

The basic sample-and-hold circuit of Fig. 2 has unity-gain bulfers to charge the capacitor without loading the signal source and to drive the next stage without changing the voltage stored. The basic operation of this circuit is illustrated in the photo-







circuit in the hold mode

high-speed acquisition systems.

during the hold mode.

graph of Fig. 3. This configuration provides fast acquisition times and is good for

The input buffer is chosen for low offset voltage, good slew rates, and the ability to drive the capacitive load. A polystyrene capacitor is used because of its very low dielectric absorption and low leakage. The output buffer needs to have a short settling time and very low input bias to prevent the discharge of the hold capacitor

The most important switch parameters are: speed, to minimize the acquisition time (fast throughput); low charge injec-

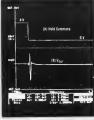


Fig. 4. Vous showing the effects of charge injection

tion, to reduce the hold step error; and low leakage, to maintain a low droop rate, The DG412 offers improvements for all three areas of performance.

The circuit shown in Fig. 2 achieved an acquisition time of under 900 ns and a droop rate of 10 µV/µs. Pedestal error was a function of analogue signal voltage. The worst-case error was 23 mV when Vin =

The photograph in Fig. 4 shows Vout immediately after the hold command. In this case, V_{in} = 0.5 V. Note the upset caused by the charge injection of the switch when it opens, the offset error that

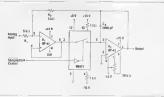


Fig. 5. Integrator output sample-and-hold lunction operates switch into virtual earth.

remains after the upset and the droop rate that begins after settling is completed.

Clased-laap integratar autput sample-and-hald circuit A popular sample-and-hold configuration

A popular sample-auto-not comparation is shown in Fig. 5. This circuit is simple and accurate. It has a gain of -1 since R₁ = R₂. Opamp A1 acts as a current booster to speed up the charging rate of hold capacitor C_H. Since the unity-gain buffer

has a very low output impedance, the time constant associated with $C_{\rm H}$ is determined primarily by the on-resistance of the switch and by the magnitude of the hold capacitor. Thus, the circuit benefits greatly from the low on-resistance of the DG411.

The settling time of the output voltage is determined by the slew rate and settling time of the integrator stage. In the sample mode of operation, the DG411 closes and hold capacitor C_H charges to the negative of the input voltage. In the hold mode, the

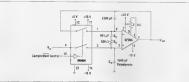


Fig. 7. Fas] and precise sample-and-hold circuit.

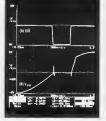


Fig. 8. V_{DUI} without compensation shows large glitches and a waveform ripple during acquisition lime.

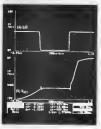


Fig. 9. Improved V_{OUT} after compensation.

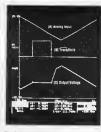


Fig. 6. Acquisition time is limited by the slew rate of the output amplifier.

analogue switch opens after the capacitor has acquired his voltage to the desired accuracy. Another advantage of the DG411 is that the switch always operates at a virtual carth potential regardless of the lapatr voltage. Since at this level the charge majection on the switch drain is at its minimized. The errors of Ai are minimized. The errors of Ai are minimized in the sample state, although they do appear in the hold mode.

The photograph in Fig. 6 shows the typical waveforms associated with this circuit. With the components shown, this circuit achieved an acquisition time of about 20 μ s, a maximum hold step error of 3.8 mV and a droop rate of 7.5 μ V/ μ s.

Fast and precise sampleand-hold circuit

The circuit shown in Fig. 7 uses a DG-630 analogue switch in conjunction with a prayr input operational amplifier. The DG-0404 is a fast switch (T_{OR}-150 ns), in this circuit, both switches have a similar potential when open, so their charge injection effect is minimized by their differential effect on the opamp. Acquisition time of this circuit was kess than 600 ns, worst-case podestal error was -5 mV, and droop rate was 35 µV/µs₁₈.

The compensation network formed by C_C and R_C helps to reduce the hold-time glitch and optimizes acquisition time. The photograph in Fig. 8 shows this circuit's output without a compensation network. Notice the large glitch going into the hold mode, as well as the rippled waveform right after the output slews to lis new value at settling time. The photograph in Fig. 9 shows the improved response after the compensating network has been installed.

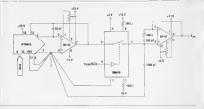


Fig. 10. Digital-to-analogue converter deglitcher.

Digital-ta-analague canverter deglitcher

Major code transitions in digital-to-analogue converters (DACs) can cause unwanted voltage spikes, commonly called glitches. In many DAC applications, these glitches can not be tolerated. Additionally, DACs from different vendors have different size glitches. (Note the glitch impulse specification on DAC data sheets). To ensure a smooth transition when the DAC goes from one voltage to the next and to guarantee uniform circuit response regardless of alternate-sourced DACs, the DAC output may be processed with a tack-and-hold as shown in Fig. 10. While the DAC input code is unchanged, the DG418 is closed and Vout tracks the output of the currentto-voltage converter. Just before a code change occurs, the analogue switch is opened so that Vout continues showing the previous voltage. After the code change and its associated glitch has settled, the DG418 closes again and the track mode is resumed.

The photograph in Fig. 11 shows V_{Out} with the DG-418 always closed (c) and with the deglitcher active (d). Notice the improvement in the transition glitches.

The DG418 offers high switching speeds, which are required for short conversion times, and low charge injection, which minimizes pedestal errors.

Dual-input programmable gain amplifier

For digital systems where only a +5 V supply is available, a small amount of analogue processing can be implemented with a low-voltage converter it and low-voltage analogue components. Figure 12 shows an amplifier suitable for data acquisition or voice recognition applications where either of two analogue signals is selected and amplified by a very precise. self-calibrating chopper-stability amplified amplified to the control of the cont



Fig. 11. Digital-to-analogue converter deglitcher waveforms.

er, Circuit gain can be selected as either x2 or x10. A single DG423 analogue switch was used to perform both the Input-select and gain-select functions. Its low on-resistance, high speed, and on-chip latches ease circuit design and improve overall accurations.

The photograph in Fig. 13 illustrates the operation of the circuit. For demonstration purposes, inputs and gain-seelest were tied together so that when the 0.5 V (p-p) triangular signal was being processed, the circuit gain was xell owhereas when the 3 V (p-p) sine wave was selected, the amplifier's gain was reduced to ×2. This type of gain ranging is useful to pre-condition analogue signals of different amplitudes prior to an analogue-to-digital conversion.

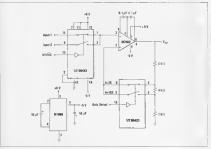


Fig. 12. Low-voltage programmable gain amplilier.

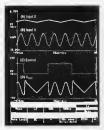


Fig. 13. Gain ranging produces similar amplitudes even if the input levels are different.

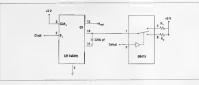


Fig. 14. Programmable one-shot multivibrator.





Fig. 15.. A logic Low produces short pulses and a logic HIGH creates long ones.

Fig. 16. This photogreph illustrates the remote switch-over action.

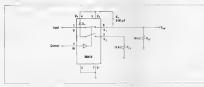


Fig. 17. Remote sept enalogue switch for switched signal powers.

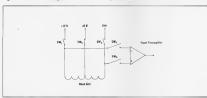


Fig. 18. DG411s in the head switching circuit of a disk drive.

10.36 elektor india october 1969

Progrommoble one-shot multivibrotor

Another useful application for an analogs switch, a programmable one-shot multivibrator, is shown in Fig. 14. This circuit produces pulses whose duration is determined by digitally selecting one of the two timing resistors—see Fig. 15. Adventages of the use of the DG419 in this circuit are:
small size (8-pin minitum or small-outline package), high speed, low on-resistance, and trit, compatibility even in single sup-ply operation.

Anologue switch powered by input signol

The analogue switch in Fig. 17 derives operating power from its Input signal, provided that the amplitude of that signal exceeds 4 V and the frequency is greater than 1 kHz. This circuit is useful when signals are to be routed to either of two remote loads. Only three conductors are required: one for the signal to be switched, one for the control signal and a common return.

A positive input pulse – sec Fig. 16 – tums on clamping diode D₁ and charges C₁. The charge stored on the capacitor is used to power the chip; operation is satisfactory because the switch requires a supply current of not greater than 1 μ A. Loading of the signal source is imperceptible. The DG4198 on resistance has the respectable value of 100 Ω for an input signal of 5 V.

Reod/write disk-drive circuit

The circuit shown in Fig. 18 allows data to be written to or read from a disk. In the write mode, SW2 is closed. A ONE is created by momentarily closing SW1. This causes current to flow in the leit-hand half of the head coil. A 27200 is produced when W3W3 is closed. This causes current to flow in the right-hand half of the coil and reverses the direction of the magnetic flux.

In the read mode, switches SW4 and SW5 are closed. This connects the head coil to the read preamplifier so that the voltages picked up by the head as the disk glides by can be amplified.

Single-supply operation with +12 V, low-on resistance and high switching speed allow an improvement in data rates of roughly ×10 when DG411s are used in place of the more mature DG211s.

Micropower ups tronsfer switch

The purpose of the uninterrupted power supply (UPS) circuit in Fig. 19 is to preserve volatile memory contents in the

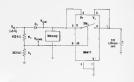


Fig. 19. Micropower ups circuit.

event of a power failure, in this application, every tenth of a volt counts. This circuit uses a micropower analogue switch that comes in an 8-pin miniotip or smalloutline package, a 3-V lithium cell to supply back-up power, a diode and two resistors. Voltage losses under 0.1 V can be achie-ved.

During normal operation, currents of several hundreds milliamperes are supplied from V_{CD}. In this mode, SWI is open, so that the only drain from the Inhium cell consists of leakage currents flowing into the V₁ and S terminals. The leakage current is typically about 10 pA. Resistors R₁ and R₂ are continuously sampling V_{CD}.

When V_{CC} drops to 3.3 V, the DG417 changes states, closing SW1 and connecting the back-up cell. Diode D₁ prevents current from leaking back towards the rest of the circuit. Current consumption by the CMOS analogue switch is around 100 pA:

this ensures that most of the available power is applied to the memory where it is really needed. In the stand-by mode, currents of some hundreds of milliamperes are sufficient to retain data.

When the +5 V supply comes back on, the potential divider senses the presence of at least 3.5 V and causes a new change of state in the analogue switch, restoring normal operation.

On-resistance is about 74 \(\Omega\) when \(V_{\text{Co}}\) is 45 \text{ V and } \(Z_{\text{Co}}\) is 43 \(V_{\text{For}}\) rexample, an 860 \(\Omega\) A load, equivalent to a static raw of 256 \(k\text{bir}\) (MCM61L16), when the produce a voltage drop of 0.1 \(V \) on the analogue switch, which is much better than the 0.6 \(V \text{drop occurring if a simple 2-diode circuit were used. \)

achieved by parallelling several sections in a multiple analogue switch such as the DG403.

Line a in the photograph in Fig. 20



Fig. 20. Oscilloscope waveforms show a cleen power switch-over.

illustrates how, in spite of V_{ex} dropping to 0 V (line b), uninterrupted power is applied to the load. Negligible voltage loss caused by the switch. Line cshows that the DG417 changes state when its control input voltage decays to 1.4 V and changes again when it reaches 1.5 V on its way back to normal. The values of R₁ and R₂ may be adjusted for different trippoints if desires.

For the applications mentioned in this erticle, the DG4090 family of silicon-gate CMOS switches comes a step closer to the ideal switch. Any application that uses industry-standard analogue switches can now be improved by choosing these fast, lower-power, versatile analogue switches.

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THE DIGITAL MODEL TRAIN - PART 6

by T. Wigmore

The sixth part in the series deals in detail with the Booster Unit.
Each of these amplitiers provides enough power for the control up to fifteen trains on a digital model track. The booster is the last unit in the series that can be used with both the Märklin and the Elektor ElectronicsDigital Train System. The units teatured in torthcoming parts in the series are peculiar to the Elektor Electronics System.

The power supply of a digitally controlled model railway track is fundamentally different from that of a conventional track, in that the supply voltage is switched rapidly between +18 V and -18 V. The switching is carried out by the booster (power amplifier).

The booster ensures that the serial control commands generated by the digital control circuits contain not only the information, but also the power to start locomotives, turnouts (points) and signals.

Since detailments, and the consequent short-circuits of the track, occur much more often on model railway tracks than on life-size ones, it is essential that the booster is provided with an efficient short-circuit protection facility.

The concept

Our booster unit has two important advantages over that from Märklin: higher output power and a regulated output voltage.

The Märklin booster provides a maximum output current of about 3 A. That is not much if you take the current drawn by one locomotive at about 700 mA, and add to this the current drawn by turnouts (points), signals, and coach lighting. It is on those considerations that our booster provides an output current of 10 A.

The output voltage of the Markin booster is fairly load-dependent: a 25% drop over the normal range of loads is quite normal. That kind of variation has, of course, an adverse effect on the speed of the locomotives and the brightness of the coach lights

The output stage is an emitter follower. Driving the bases by a voltage source ensures a virtually constant output voltage, which results in independent speed control of the trains and constant brightness of the various lights. These properties are illustrated in Fig. 39 and Fig. 41.

The use of an emitter follower also enables higher switching speeds since the transistors operate on the linear part of their characteristics: the switching times are, therefore, not adversely affected by saturation effects.

A drawback of the configuration is the higher voltage and the consequent greater dissipation in the output transistors. Fortunately, this is easily rectified by the use of somewhat larger heat sinks.

The circuit

Since the switching pattern of the track voltage contains control information, it is important that the booster provides a clean output signal. Much attention has, therefore, been paid to the switching speed. The practical outcome is illustrated in Fig. 40.

The bases of the emitter follower, Ti-Ti in Fig. 42, are switched by 17 and 76 respectively between 4:0 V and -20 V. These voltages are provided by ICi-Do and ICi-Di respectively. The final output voltage is the difference between the base voltage and the sum of the base-emitter potential (about 1.5 V) of the output transistors and the drop across the emitter resistors (maximum 0.6 V). In practice, the

output voltage is a reasonably constant ±18 V. See also the load characteristic in Fig. 41.

The emitter follower ensures a better bandwidth and regulation with complex loads than, for instance, feedback.

Emitter resistors R12-R15 ensure an equal division of current to T1-T2 on the one hand and to T3-T4 on the other.

Resistors R12 and R14 serve to measure the current in aid of short-circuit protection transistors T9 and T10. When the emitter current of T1 or T3 tends to become too high, the drop across R12 or R14 rises sufficiently to switch on T9 or T10. This causes a reduction in the base current of the output transistors and, consequently, in their collector and emitter currents.

The input stage is formed by T7 and T8 and is configured in a manner that makes a symmetrical input signal essential. If the input (pin 4 of KI) is 0 V or not connected,

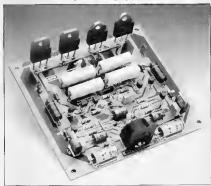


Fig. 38. The booster unit without heat sinks and enclosure.



Fig. 39. Dala Iransfer by switching the supply vollage. It is evident that the Marklin Booster (upper trace) does not provide a regulated output in contrast to the Elektor Electronics unit (lower trace).

all transistors are switched off and the output presents a high impedance (that is, no voltage is supplied to the rails). When the input voltage is between +5 V and +20 V, T7, T3, T3, and T2 conduct and the output is switched to +18 V. With the input voltage between -5 V and -20 V, T8, T6, T3 and T1 conduct and the output voltage is switched to +18 V.

All transisturs, except TS and T6, operate on the linear part of their characterstress Transistors TS and T6 are switched in the saturation region because switching transistors for voltages of 50 V and more are not available. Nevertheless, C8 ensures

that these transistors switch at a sufficiently high speed.

Overload signal

The circuit around Tn serves to indicate an overload condition. Note that only the negative output voltage is monitored. This is sufficient since the load on the negative line is slightly higher than that on the positive rail. For instance, the turnout (points) decoders work with half-wave returned and, therefore, head only the negative rail. And the control of th

The output voltage will then drop significantly and this causes a rise in the voltage and cantly and this causes a rise in the voltage carosis the output transistors and thus the dissipation. If this situation is allowed to persist, there is a danger of the booster being thermally overloaded: the consequent risk of fire is a very real one.

Therefore, if the output voltage drops

below 15 V, Tn will switch off. The signal at pin 5 of K, aided by the pull-up resistor on the main ren of the Elektor Electronics system, goes low and this results in the removal of the drive to the booster with the aid of the software. Thermal overloads are, therefore, prevented, moreover, the system 'knows' that in this condition no data can be transmitted (even if they

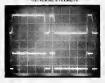
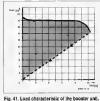


Fig. 40. Comparison of the switching behaviour under load of the Marklin Booster (upper traces) and the Elektor Electronics unit (lower freces).



could, they would not reach the decoders).

Capacitor C7 enables the overload action to be delayed, so that the system is not disabled at every momentary short circuit. This will be reverted to later in the series.

Construction

If the PCB shown in Fig. 45 is used, construction of the booster unit should not present any problems.

Fit the wire links first those close to the output transistors should be of 1 mm dia. wire

Mount resistors R12-R15

well away from the board, because they get pretty hot during operation.

The board has provision

The Board has provisions for a 5-pin DN connector, but if the booster is intended for use in a stationary position (which is normally the case), the respective wires may be soldered direct to the board.

Circuits IC1 and IC2 do

Circuits IC1 a not need a heat sink

Do not fit C7 at this stage.

Transistors T1-T4 must be mounted on a heat sink with a thermal resistance of not less than 0.8 K/W with the aid of good-quality insulating

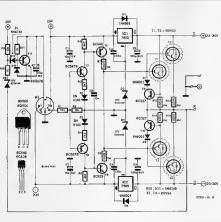


Fig. 42. Circuit diagram of the booster unit.

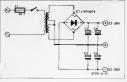


Fig. 43. Circuit diagram of a recommended power supply.

22 - 30V

Fig. 44. If you are content (for the lime being) with a much smaller output current, this power supply will do nicely.

capacitors is 225-29 V. If you measure 0 V, it is almost certain that the two secondary windings have been connected in anti-phase. Switch off the mains, discharge the capacitors via a resistor and reverse the connections of one of the secondary windings. Then check the direct voltage again.

If everything is all right, switch off the mains again and discharge the buffer capacitors via a resistor.

Next, connect the supply to the booster via insulated wire of at least 0.5 mm dia. and switch on the mains. Check that the

Assembly and test

Since the booster is operated from the mains, great care and attention must be paid to correct assembly and insulation. Because there are always metal parts in a model railway system that can be touched (like the rails), it is advisable to use a good-quality insulated enclosure.

The insulation of the power supply transformer stated in the parts list is approved to Class I. This means that the mains cable should have three cores, one of which is earth.

All metal parts that can be touched (including the heat sinks) should be connected to earth.

Connect the two secondary windings of the mains transformer in Fig. 43 in series and fit and solder the rectifier and the buffer capacitors (Cloi = C1 + C2 = C3 + C4 = $\geq 20,000 \, \mu F$ rated at $\geq 40 \, V$). Before the supply is connected to the

booster, switch on the mains and check that the direct voltage across the buffer

Parts list

Resistors: R1;R2 = 18 k R3;R4 = 2k2 R5;R6 = 4k7 R7;R1 = 1000;1 W R8 = 10k R10;R11 = 1k0 R12(196R15 = 00,15;4 W

Capacitors: C1;C2 = 10µ; 25 V C3;C4 = 220n C6;C6 = 100µ; 40 V C7 = 68µ; 16 V C8 = 10n

Semiconductors: D1;D2;D10;D11 = 1N4148 D3;D4;De = zener dlode 15 V; 400 mW D5-Ds = 1N4001

T1;T2 = BDV 65 (Philips Components)
T3;T4 = BDV 64 (Philips Components)
T5 = BC640

Te = BC639 Tr = BC547B Ta = BC557B

Te = BC557B Te = BC337 Tio = BC327 Tii = BC557

T11 = BC557 IC1 = 7805 IC2 = 7905

Miscellaneous: K1 = 5-way DIN socket (180°) for PCB

mounting.
5 off car-type spade terminals for PCB mounting.

insulation material for T1-T4
PCB Type 87291-6

Recommended power supply parts (not on PCB):

Mains transformer: 2x18 V @300 VA (e.g. ILP 73014)

Smoothing capacitors: 4 off 10,000µF; 40 V or 4 off 15,000µF; 40 V.

High-current bridge rectifier: min. 20 A (e.g., BYW61 from Motorola).

One mains-rated fuse: 2 A slow.

One mains-rated fuse: 2 A slow.
Two low-voltage fuses: 10 A fast .
Heat-sink; e.g., SK120-100mm (Dau Components; Fischer).

washers. If BDX66/67 darlingtons (with TO-3 housing) are used, they must first be

Power supply
The circuit diagram of a recommended
power supply is shown in Fig 43. The
2×18 V transformer must preferably be a
toroidal type. The rectifier must be a
heavy-dut type and needs a heat sink (it

mounted on to the heat sink and then con-

nected to the board by not too long, heavy-

duty wires.

may be mounted on to that for Ti-Ta). If you do not want to go to the expense of a new transformer, but rather use one that you have had lying around for some time, use the circuit shown in Fig. 44 Remember, however, that such a set-up will normally not be able to deliver more than a quarter of the power of the supply in Fig. 33. If that.

Finally, DO NOT connect transformers in parallel to increase the total available current: such a set-up can be a death trap.

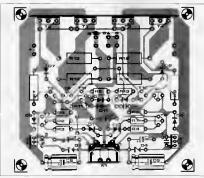


Fig. 45. Printed circuit board for the booster unit.

output voltage of IC1 is +20 V and that of IC2 is -20 V. There should be no voltage between B (earth) and R since there is as yet no input

Fit a 100 Ω , 5 W, resistor between B and R and connect the input, pin 4 of K₁, to a positive voltage, for instance, +20 V at pin 3 of K₁. The output voltage should then be +18 V. With a negative input - obtained by interconnecting plns 1 and 4 of K₁ - the output should be -18 V.

Connecting to Mörklin Digital

The booster circuit is driven via K1, which also carries the auxiliary +20 V and -20 V voltages. These are not of importance when the Marklin Digital is used, but in the Elektor Electronics system they power the RS232 interface.

When the Marklin Digital is used, only pins 2 (earth) and 4 (input) of Kt need to be connected to the brown and red terminal at the rear of the Central Unit. Our booster, therefore, does NOT use the 5-pin connector on the Central Unit.

The overload signal (pin 5 of Ki) is also for use with our own system only. To arrange for the automatic switch-off of the Mārklin unit during overloads, a diode must be added as shown in Fig. 46. Warning of a short circuit in the booster is then passed to the Central Unit, after which the current monitor in that unit arranges the switch-off.

The Central Unit may provide some of the power to the rails, but note that only the B connexions of the Central Unit and our booster may be interlinked. The R con-

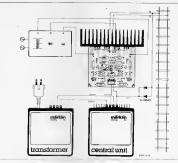


Fig. 46. How to connect the booster unit to Marklin's Central Unit.

nexions (centre rail in the Marklin system) must be isolated from one another. Marklin supplies special parts to prevent the slide contacts from short-circuiting the electrically separated centre rails during cross-overs.

For true-to-scale modellers
The output voltage of the booster was cho-

sen at \$118 V to ensure that the maximum speed of the locomotives would be about the about to that in traditional model railway systems. Taken to scale, model trains travel faster than life-size ones. Modellers who want to have their locomotives travel at, at trains can arrange their locomotives travel at, at trains can arrange this by using \$12 V zener trains can arrange this by using \$12 V zener than the proportionally.

NEW PRODUCTS

AUTO TEST SYSTEM FOR POWER SUPPLIES

The Chroma 6000 Power Suppy Auto Test System, nanutactured by Chroma ATE Inc., Taiwan, is used for testing power supplies, both AC/DC and DC/ DC types. It includes Switcher Analyzers, Vin Sources, an Extended Measurement Unit and a System Controller (IBM PC-XT or compatible). The modular hardware configuration allows the Switcher Analyzer notable into the Chroma 6000 Power Supply ATS by incrementing hardware modules.

The Chroma-6000 ATS offers a MULTI-SYSTEM and PARALLEL Iseling architecture to improve the test efficiency and accuracy. Each of the sub-system and the Extended Measurement Unit, contains a CPU, memory, dedicated control and measurement circuits, which is capable of distributed processing during test



execution. The Chroma 6000 ATS software packages provide a powerful menu driven, programmer free operation.

A.T.E. LIMITED • (Electronics Division) • 36, SDF 2 • SEEPZ Andheri (East) • Bombay-400 096.

Infra Red Pyrometers

L & Tis marketings non-contact temporature measuring systems havings wide applications is steel, cement, glass, heat treatment, bitumen mixings, food processings etc. These systems use infra red radiation technology and are manufactured by Hozur Instruments Privale Ltd. in collaboration with hand Infrared Ltd. of U.K.



Larsen & Toubro Ltd. • Process Instruments Division • Venkata remanna Centre • Madras-600 018 •

RESONANCE METER

The test instrument discussed is a must for anyone working with RF signals, but with a limited budget. It enables the resonance frequency of tuned circuits to be measured within the range of 100 kHz to about 50 MHz, and can also be used as a capacitance meter, RF test generator and RF signal probe.

J. Bareford

Traditionally, the name of the instrument of the type to be described has evolved from grid dipper to gate dipper or simply dipper. The first name, grid dipper, was used in the valve era and long after. When thermionic valves disappeared from consumer electronic equipment, the instrument was built from semiconductors and

baptized 'gate dipper' because the gate of a field effect transistor (FET) is electrically very similar to the first grid of a valve. The instrument is basically an RF signal source with adjustable output frequency, coupled to a circuit that measures and indicates the amplitude of the output signal — see Fig. 1. Because the terms 'gate'

and 'grid' have been formed historically, but have really nothing to do with the basic function of the instrument, these misnomers are omitted here to be replaced by the more universal term 'resonance meter'.

Tuned circuits and resonance

Many constructors shy away from prosects that contain home made inductors. because these, they feel, remain something of a mystery owing to their lack of experience or suitable test and measuring equipment. And yet, many a radio amateur will confidently inform these constructors that there is nothing mysterious about winding coils. In fact, dimensioning them and peaking the resultant tuned circust at the right frequency is sheer pleasure, provided, he will tell you, that a resonance meter is available. Without this simple instrument even experienced RF engineers are often at a loss in getting radio equipment to work correctly.

Any tuned circuit absorbs energy from another that is placed near it, and resonates at the same frequency. The RF energy is supplied by the resonance meter and an inductor that forms part of an oscillator. When this inductor is held near the coil under test, the oscillator output amplified the same frequency. When the dip between the coil to the control of the con



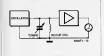


Fig. 1. Block diagram of the resonance meter.

the resumance frequency can be determined while the equipment of which the buned circuit forms part is not powered. The coupling between the resonance meter and the tuned circuit under test is noted to be a superior of the coupling of the hold the coupling of the LC network under test.

Resanance meter as an RF signal saurce...

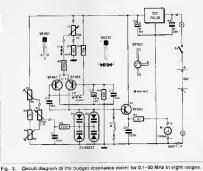
Since the resonance meter contains a nociliator capable of covering a fairly large frequency range, it may double as an RF signal generator. To align a receiver, for instance, the resonance meter is simply set to the required frequency and placed close to the aerial input. If it is too strong for a precise adjustment, the test signal can be attenuated by placing the resonance meter further away.

... as a frequency meter or RF probe...

The resonance meter is designed such that it can easily be used as a coarse frequency meter and signal strength meter (RF probe). These functions are achieved by switching of the internal oscillator, but leaving the pick-up coil and the signal rectifier plus level indicator in function. Energy picked up from a resonating, in-

f (MHz)	L (H)
0.1-0.2	10m
0.2-0.45	2m2
0 45-1.0	470μ
1.0-2.0	100μ
2.0-4.5	22μ
4 5-10	4μ7
10-20	1μ
15-40	0μ22

Table 1. The values of Ls.



Tig. 1. Oneon angular of the angular

ductor in equipment to be aligned thus causes the meter to deflect when the tuning dial is set to the correct frequency. The meter indexion is a measure of the signal strength, while the tuning dial shows the measured frequency. These combined functions are particularly useful for aligning receivers and transmitters. The probefunction of the resonance meter is then classified in the control of the control of the control of the control of the resonance meter is then classified in the control of the resonance meter is then classified in the control of the c

...and a C ar L meter

Capacitance (C) and inductance (L) measurements are the last additional functions of the resonance meter.

The value of a capacitor can be determined with the aid of a parallel inductor with known inductance, L, and, of course, a resonance meter. The capacitance, C, is simple to calculate from the resonance frequency, fo, of the parallel tuned circuit:

$$f_0 = \frac{1}{2 \pi \sqrt{LC}}$$

Since the self-inductance is known, and the resonance frequency can be measured, the equation can be rewritten as

$$C = \frac{1}{40 \, \text{fb } I}$$

Similarly, inductance can be calculated with the aid of a reference capacitor:

$$L = \frac{1}{40 \, f_0^2 \, C}$$

Three tronsistars

The circuit diagram of the resonance meter is given in Fig. 2. All functions discussed above are realized by three transistors and a handful of passive components. Although perhaps a little difficult to deduce from the circuit diagram, I and Ti form an oscillator. The frequency of oscillation is determined by Ls and varicaps Di and Di. The two diodes are connected in parallel to achieve the required capacitance range that can be adjusted with Pi. A total of eight plugic inductors is

A total of eight plug-in inductors is required to cover the frequency range from 0.1 to 50 MHz.

Preset P2 allows the collector current in both transistors to be adjusted, giving control over the amount of RF energy generated by the oscillator. Transistors Ti and Ti form a differential amplifier in which C2 provides the feedback between the collector of T2 and the base of T1.

The measuring amplifier is formed by Ts. This transistor is operated in class C so that it does not conduct until the voltage on L3 is about 0.6 V higher than the emitter voltage. This means that T3 forms a basic rectifier because it conducts only during a part of the positive half-wave of the oscillator signal. This pulsating signal is converted into a clean direct voltage by C4. Regulator IC: prevents fluctuations of the supply voltage degrading the stability of the oscillator. Should the supply voltage be unstable, the voltage at P1, and with it the varicap voltage, is unstable also. The varicap voltage, by the way, is not only dependent on the setting of P1. Presets P3 and P4 are included to give P1 the correct range, which is a must for the calibration of the scale on the front-panel designed

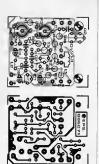


Fig. 3. Printed-circuit board for the resonance meter.



for the resonance meter. The ranges of the resonance meter can only be calibrated if the standard choke values listed in Table 1 are used.

The circuit diagram shows that the supply voltage for the resonance meter is 18 V, obtained from two series-connected 9 V batteries. A mains adaptor with 12 VDC output is, however, also suitable if the resonance meter is fitted with a Type 78L10 voltage regulator.

Construction

Resonance meters for frequencies up into the VHF range are not the easiest of construction projects. The main problem of many home-made as well as ready-made meters is that these produce false dips when the pick-up coil is not hidd near a tuned circuit. According to Murphy's law, these false dips will typically occur in the most frequently used ranges.





Fig. 4. True-size front-panel layout.

8 off DIN-type 2-way loudspeaker plugs.

The printed-circuit board for the present resonance meter has been designed to minimize the risk of false dips. Figure 3 shows the component mounting plan and the track layout of the board, which is available ready-made.

Mounting the parts on the board is fairly straightforward. The only point to pay special attention to is that all component wires must be kept as short as possible.

The populated board is mounted in an ABS enclosure. This is not standard practice in view of RF screening, but avoids the risk of a metal enclosure affecting the operation of the oscillation. As a result, false dips would occur, and the calibration would have to be changed.

All wires in the enclosure, and particularly those between the board an the inductor socket should have the absolute minimum length. The front-panel design shown in Fig. 4 is copied and secured on to the enclosure.

The pick-up coils are made from DIN-

type 2-way loudspeaker plugs and readymade chokes as shown in the photograph of Fig. 5. The chokes for the two lowest ranges must be types with plastic sleeving, not types with ferrite encapsulation. The other chokes are miniature axial types.

Calibration

The resonance meter can not be calibrated before it has been fitted into a suitable enclosure. Either a frequency meter or a short-wave receiver must be used for the adjustment procedure.

If a frequency meter is available, the procedure is started by winding 10 turns of enamelled copper wire on to a lead pencil. Remove the pencil, and connect the inductor to the input of the frequency meter. Plug one of the lower-range coils into the resonance meter, switch on the Instrument, and adjust P2 for full-scale deflection of the signal level meter, M1. The frequency meter will display a frequency if the pick-up coil on the resonance meter is held near that on the frequency meter. Check whether the displayed frequency rises if P1 is turned anti-clockwise. If not, swap the outer wires on the potentiometer. Set the tuning to the highest frequency in the range, and adjust P3 until the frequency meter displays the scale frequency. Turn P1 to the lowest frequency, and adjust P4 similarly. Once again check the upper frequency and correct the setting of Ps if necessary.

A short-wave receiver is also suitable for calibrating the resonance meter, but has the disadvantage of requiring to be re-tuned for every adjustment.

Since every choke has its particular tolerance, it is necessary to check for scale deviations in every range of the resonance meter. If the deviation in a particular range is unacceptable, try using another choke from another batch but with the same value indication. Choke tolerance is typically #20%.



Practical use

The resonance meter is a test instrument that becomes easy to operate only gradually through regular practical use. Prior to any measurement, the frequency range must be determined, and the appropriate pick-up coil selected. In some cases, you will need to change coils if the resonance frequency is close to the end of the range. Switch on the instrument, and adjust the sensitivity control, P2, for f.s.d. (full-scale deflection) of the signal level meter. Line up the pick-up coil with the inductor in the equipment (Fig. 6), and tune carefully until the pointer of the level meter moves to the left. The frequency range is probably fairly large at this stage. To achieve a more accurate dip, move the pick-up coil away from the inductor while still ensuring that they point in the same direction.

Now retune the resonance meter until a sharp dip is found.

If the resonance frequency of a tuned circuit is not known, it is wise to start examining it in the lowest range of the resonance meter, increasing the range until a sharp dip is found. This procedure avoids harmonics being mistaken for the natural frequency.

The resonance meter need not be very accurate since its main application is the coarse dimensioning and adjustment of inductors, or capacitors that form part of an I-C tuned circuit — precise adjustment is invariably done along the lines of the setting-up procedure with the equipment turned on Also, it is useful to note that the resonance frequency of an I-C circuit is esperally lowered when it is installed in the circuit, which introduces additional capacitance.

Not all tuned circuits can be tested with the aid of the resonance meter. Inductors wound on a toroid core, or enclosed by a metal cover, absorb very little externally applied energy, and do not produce a dip unless a small external series inductor of one or two turns is added temporarlly. This lowers the resonance frequency to some extent, but allows a useful estimate to be made. Some in-circuit L-C networks will not dip either. Examples are the heavily damped tuned circuits in the emitter line of a grounded-base transistor circuit. To measure the resonance frequency, either the transistor or the tuned circuit must be removed.

Finally, the resonance frequency of series L-C tuned circuits can not be measured unless a capacitor is included in the circuit that provides a path from the inductor back to the series capacitor. This, in fact, creates a parallel tuned circuit.

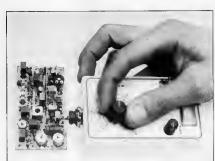


Fig. 6. Using the resonance meter to 'dip' an $\emph{L-C}$ tuned circuit.

CENTRONICS MONITOR

A. Rigby

The Centronics interface standard is often said to be without problems in practical use. When a malfunction occurs, however, many more connections have to be checked than, for instance, on an RS-232 link. The monitor described here alleviates the plight in debugging a Centronics connection. It is a handy tester that indicates the levels on all lines simultaneously, including those that carry pulses.

Nearly all of today's personal computers are equipped with a Centronic port for connecting a printer. The general acceptance of the Centronics interface standard has been helped by the availability of ready-made cabbes of various lengths, and the fact that the majority of printer manificturers have ensured compliance with the pinning of the 'blue-ribbon' input connector on their products.

Sometimes, however, the installation of a new printer or cable gives rise to awkward problems that take a lot of preclous time to analyse and resolve. In these cases, the present in-line indicator provides almost instant fault analysis because it shows the logic state of the databits and a number of handshaking and control signals.

Data and handshaking

To ensure that the computer-to-printer link works as required, a number of signals must be present, while the use of others depends on the equipment used at either side of the Centronics cable. At the computer side, datalines D0-D7 must be

connected, as well as handshake lines STROBE, BUSY and/or ACK (acknowledge). Especially the last two signals are prone to cause trouble if the relevant pins are correctly marked (according to the printer manual), but not used electrically.

When the Centronics connection is fully functional, the computer puts the bit pattern to be sent to the printer on to the eight datalines, and actuates the STROBE line by pulling it low. This enables the printer to recognize that the databyte representing the printable character is stable and therefore valid. Reception of the byte is signalled to the computer by a low-tohigh change on the BUSY line. BUSY remains high until the printer is ready. Depending on the type of printer, the received databyte is instantly printed, or stored in an internal buffer memory. In both cases, however, the processing (which is not necessarily the same as printing) of a character is signalled to the computer by means of a high-to-low transition on the ACK line. The processing of received characters

differs from printer to printer. Older models print each character immediately after it has been received, halting the computer during the printing operation. Printers of a later generation typically feature a small buffer that allows a line of printable characters to be stored. The characters in this cut in the printing of the control of the characters in this manner of the control of the control of the characters in this printers have buffers capable of storing many kilohystes of text, and handle printing, data spooling and communication with the computer simultaneously. Some top-range models house more data processing chips than the average PC com-

Apart form the data and handshaking lines, the Centronics standard specifies a number of other, auxiliary, functions:

Paper Empty Goes high when the printer is out of paper.

printer is on line
and ready to receive data.

AUTO Auto Feed Automatic line

INIT Initialize

feed after a carriage return. Resets the printer Indicates internal failure.

The last four lines must be given a fixed level, even if they are not used in the actual connection between the computer and the printer. In other words: the minimum requirement is that non-connected active-low and active-high lines be fitted with a pull-up and pull-down resistor respectively.

The monitor

The Centronics monitor indicates the current logic level on all lines by means of light-emitting diodes (LEDs). The databus lines are connected to a Type 74HCT540 buffer that supplies sufficient output current to connect the LEDs direct to ground. A logic high level causes the LED assocition of the control of the control of the theory acts lines is connected direct to the associated LED. This can be done with impurity because the signal elvels are



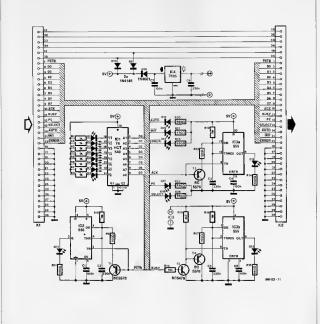


Fig. 1. Circuit diagram of the Centronics monitor.

fairly steady. Signal lines STROBE, BUSY and ACK require a different configuration because they carry pulses rather than steady levels. Three monostables in the form of Type 555 timer chips are therefore used to drive the relevant LEDs. Inverter Ta-Ris-Rie ensures that the BUSY LED lights when the associated line is actuated (i.e., logic high). Such an inverter is not required for the ACK and STROBE lines, which are active-low. The associated 555s are housed in dual timer ICs, a 556.

All other signals that may be available, but are not strictly required for correct operation, are simply passed between the relevant pins of the input and output socket of the monitor. Many Centronics cables do not have separate ground wires, but use commoned connector pins at both ends. These puns are often connected by a single wire

Sixteen LEDs enable the user of the monitor to locate the possible source of trouble at a glance: 8 data LEDs, 3 for the handshaking lines, and 5 for the status lines.

Power supply

An external supply will not be required in most cases because virtually all modern printers supply +5 V at pin 18, 35 or both. Diodes Do and Do ensure compatibility of the monitor with these printers, and also allow the unit to be powered from an external 10 V/50 mA power supply. Regulator IC+ then provides the 5 V supply voltage for the ICs and LEDs on the board

Connections

Connector Ki is a 36-way Centronics socket with straight solder pins. Push the socket do to the PCB-edge, while ensuring that the pins align with the copper standars. Soldering is then straightforward. Connector Ki is removed from a standard Centrolic solde plug, and secured as Ki. Two types of connector exist versions with change for the screws and versions with change for the screws and versions with change for the screw rape read that the property of the screw type is the better for the present application.

Pin	Signal	Source
1	STROBE	Computer
2	Data 0	Computer
9	Data 6	Computer
1	Data 2	Computer
9	Data 3	Computer
9	Data 0	Computer
7	Data 5	Computer
9	Data 6	Computer
9	Data 7	Computer
15	ACK	Printer
11	BUSY	Printer
12	PAPER EMPTY	Printer
13	SELECT	Printer
14	AUTO FEED XT	Computer
15	n.c.	
15	ground	
17	chassis	
18	+5 V	Printer
15	ground	
20	ground	
21	ground	
22	ground	
23	ground	
24	ground	
25	ground	
26	ground	
27	ground	
28	ground	
29	ground	
30	ground	
31	INIT	Computer
32	ERROR	Printer
33	n c.	
34	n.c.	
35	+5 V	Printer

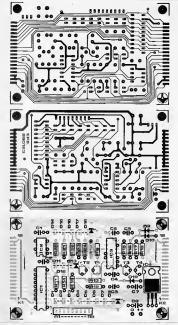


Fig. 2. Track leyout and component mounting plan. A number of perts must be soldered at both sides of the printed-circuit board.

Resistors (±5%): R1-R6 = 1k0 SiL resistor array R1-R19-R24 = 680Ω R9-R12/R17 = 100Ω R10/R13/R18 = 1M0

R15 = 10k R16 = 4k7

Capacitors: C1;C4,C6;C7 = 100n C2:C3:C6:C8 = 330n

Semiconductors: 01-De;D11-D16 = LED; 3 mm; red Ds;D10 = 1N4148 D10 = 1N4001 T1;T2;T4 = 8C557B T3 = 8C547B IC1 = 74HCT540 IC2 = 555

IC3 = 556 IC4 = 7805 Miscellaneous:

K₁ = 35-way Centronics socket with straight solder pins. K₂ = 36-way Centronics plug.

Enclosure: e.g., OKW model A9407113. PCB Type 890123

ASIC MICROCONTROLLERS

by Simon Young*

This article discusses the evolution of the MCS-51 architecture and how to use ASIC technology to extend the set of generic features contained in the family members.

Intel offers the MCS-51 architecture to customers in a number of ways

The first is via standard products, such as the 80C5JBH and 8052. These devices are designed for the general microcontroller market, where the internal hardware resources can be closely matched to the system requirements.

The second is via Application Specific Standard Products (ASSP) developed for a vertical market sharing a common set of additional features. An example is the 80CS1FA, which augments the MCS-51 core features with a programmable counter array, an enhanced serial port for multiprocessor communications and an up/down timer/counter. The third way to gain access to the

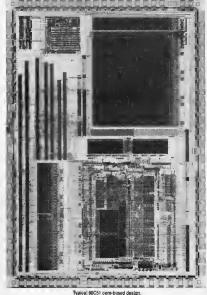
MCS-51 architecture is via ASIC, and this is the subject of this article. Intel offers to customers the same capability it uses in house to develop ASSPS.

MCS-51 Microcontrollers The MCS-51 family of microcontrollers

was designed to meet the needs of embedded control applications. The architecture and instruction set were optimized for the movement of data between internal memory and internal peripherals.

Figure Ia shows the MCS-51 architecture. The Special Function Register (SPR) bus connects the internal resources (such as port latches, timers and peripheral control registers) with the CPU. The 128 bytes of ont-tilp RAM (between 00 hex and 7F hex) can be addressed both with direct (MOV data addrs and indirect (MOV @RIS) addressing modes. Some devices, e.g., the 8052, provide an additional 128 bytes of on-thip RAM for temporary data storage between 80 hex and FF hex (dotted in Fig. 1b). This may be addressed only indirectly – forming a useful area for the stack.

The SFR space appears to the CPU as 128 bytes of memory located between 80 hex and FF hex. This area of memory is accessed only by direct addressing modes, in order to distinguish it from the addition-



Typical bucs I core-based design

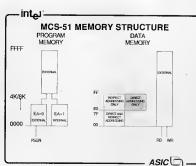
al data RAM discussed above. Of the 128 locations, 21 are used in the 80C51BH standard product (26 on the 8052).

The 64 Kbytes of external data memory space are accessed with the MOVX instruction.

Another powerful feature of the MCS-51 architecture is the ability to address individual bits within certain SFR and internal RAM locations. All MCS-51 devices contain a complete Boolean (single-bit) processor. The MCS-Si instruction set supports the Boolean processor with instructions to move, set, clear, complement, ox, AND, and conditional branch on bit. This 'bit addressability' allows individual bits to be tested and modified without the need of complex masking operations, with consequent significant

improvements in speed.

^{*}Simon Young is with Intel Corporation (UK) Ltd at Swindon



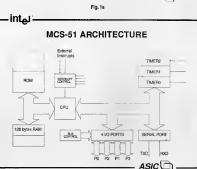


Fig. 1b

At the time the first members of the MCS-51 family were introduced, there was no economic packaging for high pincount devices. The parts were packaged in 40-pin DI, packages only recently have PLCC packages been used. To provide access to the internal hardware resources of the device, several functions, including port input and output signals, external multiplexed address/data bus, serial port i/o, external interrupt signals and timer/counter imput signals had to be multiplexed. Clearly, functions multiplexed on the same pin may not be used concurrently.

As systems designers developed increasingly complex embedded control applications, the 805! required additional memory, peripherals and/or 1/o ports. These had to be added externally as memory or memory-mapped peripherals, reducing the parallel 1/d available on the 8051. Fully expanded in this way, only a single 8-bit ty opor is available. While the on-chip features and price-performance ratio of the 805 make it still an attractive proposition when compared with other solutions, the end result is different from what the 8051 was designed to be: a single-chip, stand alone microcontroller.

UC51: Intel's original microcontroller core

In 1985, Intel introduced the UC51, which was developed from the 1.5 µm CHMOS III 80C51BH standard product. The UC51 allows designers to integrate the microcontroller core, memory, memory-mapped peripherals and cells from the 1.5 µm standard cell library on to a single chin.

In transforming the 80C51BH into the UC51 core cell, the t/o pads and pin multiplexers were removed. The internal peripherals, multiplexed address-data bus, control signals and input and output ports all have dedicated signals.

With the ability to choose different amounts of program ROM (zero, 4 K, 8 K or 16 K bytes) and data RAM (up to 1 K bytes) with no loss in functionality, the UC51 has been a very successful part of lnnel's Astc offering.

In summary, the UCS1 provides systems designers the capability to integrate a "fixed" core and memory-mapped peripherals, complete with user-defined logic, on to a single ASI device. The ASI resembles an integrated version of the discrete solition, with increased flexibility because of the demultiplexed //o. However, it is not possible to apply the full power of the architecture and instruction set to memory-mapped peripherals.

UCS51: Intel's next generation microcontroller core

Intel have recently introduced the UCS51 analy of microcontroller and peripheral cells into the 1.5 µm CHMOS II STATE CHILD THE AND THE METALLY THE UCS51 permits systems designers to connect any of the available peripheral cells or user-defined logic directly into the SFR space. The UCS51 cores then access the control registers within these peripherals in caucity the same way as any internal SFR register. There are great benefits to be gained

from directly connecting peripherals to the SFR bus:

- instructions operating on peripheral registers in the STR space are more codeefficient then accessing memory-mapped registers indirectly (with MOVX), so that less program memory space is required;
 registers/instructions/movements/instructions/ registers/instructions/movements/
- register-direct-instructions (ADD, ADDC, SUBB, INC, DEC, ANL., ORL, XRL, MOV, PUSH, POP, XCH, CINE and DINZ) execute more quickly, giving improved system throughput;
- certain bytes in the SFR space (located at X0 hex and x8 hex) are bit addressable; mapping peripherals into these locations permits the bit-banging capabilities of the Boolean processor to be applied to these registers;

interface logic between the UCS51 core and UCS51 peripherals is eliminated: there is no need of an address latch, address decoder or tri-state bus driver.

The basic UCS31 core cell resembles a UCS1, north has been removed to provide access to the ser bus, although it may be replaced easily as described later. Interfaces have been added for connecting 60M modules (either none or one of 4 K, 8 K, or 16 K bytes), a RAM module (same AMA as 8052) and an interrupt expansion unit. A functional cell diagram is shown in Fig. 2.

Additional interrupts enhance real-time performance

Unexpanded UCS51 cores have five interrup signals available, as have the UCS1 and 80CS1BH. Users may configure the internal peripheral interrupts for use as general purpose interrupt signals, with no change in priority levels and vector locations. It is also possible, by the use of the interrupt Expansion Unit, to add a further five external interrupts, making a total of 10, with complete flexibility of interrupt source, peripherals, on-chip or off-chip logic.

unique microcontroller cells

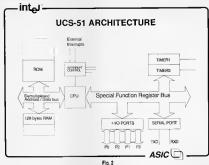
The Bus Interface Unit is, perhaps, the most important UCS51 peripheral cell. Functionally, it is and 8-bit input, 8-bit output 5FR bus interface. With it, designers may replace FORT1 and add further demultiplexed I/O ports as needed.

This cell is also used to interface between on-chip user-defined logic and the SFR bus. Thus, customer developed logic using cells from the 1.5 µm standard cell library may be mapped directly into the SFR space to gain the advantages discussed previously.

The 8-bit, 8-channel successive approximation ADC has a nominal conversion speed of 20 µs at a core frequency of 16 MHz. A conversion may be triggered by hardware or software, with an interrupt generated on completion.

Timer2 is a 16-bit timer/counter cell, enhanced over the Timer2 found on the 8052 standard product and some ASSPS.

The serial \dot{V} 0 cell is a full-duplex serial port, enhanced from the serial channel contained in the 80C51BH by the addition of a new mode. Mode 4. This mode provides 9-, 10-, 11- or 12-bit transfers with variable baud rate. In Mode 4, the UCS51SIO cell also generates partly for transmission and detects framing, overrun and parity errors on reception.



ig. 2

The baud rate generator cell is used to generate clocks for the serial 1/0 peripheral or for user-defined logic. Operating from the 16 MHz system clock, the BRG generates rates from 50 Hz to 4 MHz with an accuracy better than 0.2%.

These five Lst peripheral cells and 16 distinct core configurations complete the UCS51 offering at the time of launch: more are in development. The 1.5 µm standard cell library includes SSI, MSI and 40 functions and may also be integrated on a UCS51-based ASIC.

CAD tools old development of microcontroller-based asics

The Design Entry Tool, DET, provides a high-level, menu-driven means of configuring the core hardware resources. The UCS51 core options are RAM, ROM or interrupts. Adding a peripheral requires two data to be entered: the peripheral type and the address of its control registers in the SFR space.

The DET outputs a symbol for this core. The designer simply adds the user-defined logic he requires, surrounds this with the l/o pads and the design capture is complete.

Once captured, the designs netlist is transmitted to bMVs — Intel's Mainframe Design Verification System based on VAX/ZyCad hardware. Full-timing gate-level simulation of the entire chip is positive to the control of the control of the control of the Chip is positive to the Chip is positive to

to the ASIC.

The simulation output may be viewed as text on the host, or returned to the workstation for display and review in the graphics condition.

The ICE-UCSS1 In Circuit Emulator allows the designer to develop and test code for a UCSS1-based Asic, and to emulate the completed Asic (core, peripherals and user-defined logic) in the target system. The ICE is a Pc-based emulator system, offering the same advanced features as Intel's other ICE systems.

The UCS51 core is tested with a slightly modified version of the 80C51BH standard product test program, guaranteeing functional and parametric equivalence to the standard part. The peripherals are tested in the same way.

The designer is responsible only for his user-defined logic, and provides TPDL and ExtASM51.

The result is standard producty quality and reliability: an AQL of 0.1% is guaranteed,

Summory

Intel's family of UCS51 core and peripheral cells provides the systems designer with unprecedented flexibility in ASIC design. Not only is access provided to the basic core architecture of the 8051, but also to a specialized set of peripheral cells. The design tools guide the designer through design capture, simulation and test vector developments. All components of the UCS51 family were developed with one overriding aim: to provide guaranteed success of UCS51-based AsIC devices.

PRACTICAL FILTER DESIGN – PART 8

by H. Baggott

The Chebishev section has one of the steepest cut-off profiles of all types of filter. Unfortunately, it also has a limiting deficiency: a ripple in the pass band. The Chebishev filter can be dimensioned in various ways: the ripple is at all times limited to a certain value. This part of the series includes the Chebishev design tables for a ripple of 0.1 dB.

The Chebishev function is one of the most effective functions for realizing a filter: it combines a pronounced bend at the cut-off point with a sharp profile. This combination also results in ringing, which, by careful design can fortunately be kept within a given value. There is, however, a direct relation between the cut off profile and the ringing; if the former is made steeper, the latter becomes more pronounced; and if the ringing is kept to a small value, the profile is less steep. In practice, a compromise is reached, be-cause in virtually all applications a ripple exceeding I dB is unacceptable. This part and Part 9 will deal with Chebishev filters with a 0.1 dB and a 0.5 dB ripple respectively. These are the values that satisfy most applications.

A general drawback of Chebishev filters is the very irregular delay time that, for instance, makes the filter unsuitable for use in loudspeaker cross-over networks.

The computation of the Chebishev poles can be done in two ways. In the first, use is made of the Chebishev polynomials, while in the second the real part of the noles of a Butterworth transfer function are multiplied with a constant factor. which results in a shifting of the poles from a circle to an ellipse. Note that in the Chebishev polynomials the cut-off point is not at -3 dB, but the tables take this into account.

Ti	abda abda	10		
	,	real part — α	imaginary part ± β	- Angel
	2	0.6074	0.7112	М
	3	0.346 0.696	0.671	1
	4	0.2174 0.5248	0.9292 0.3849	I
	6	0.1466 0.3636 0.4744	0.8565 0.5912	
	6	0.1049 0.2885 0.3913	0.9716 0.7112 0.2603	
	7	0.07846 0.2198 0.3177 0.3526	0.9606 0.7883 0.4384	1
	8	0.06079 0.1731 0.2591 0.3056	0.9664 0.8353 0.5586 0.1852	
	9	0.04844	0.9905 0.871	

0.2248Table 10. Pole locations of Chebishev filters with 0.1 dB ripple.

0.4566 0.1573

Table	Table 11									
n	C1	L1	C2	L2	C3	L3	C4	1.4	C5	L6
2 3 4 6 6 7 8 8	0.06908 0.226 0.06999 0.2071 0.05584 0.2006 0.06433 0.1981 0.06363	0.488 0.2638 0.5136 0.2476 0.4883 0.2418 0.4779 0.239 0.4729	0.266 0.1539 0.3567 0.1524 0.3564 0.1498 0.3538 0.1484	0.4546 0.2476 0.5808 0.2674 0.5876 0.2878 0.5833	0.2071 0.1559 0.3564 0.161 0.3854 0.1606	0.4448 0.2418 0.5987 0.2878 0.6036	0.2008 0.1584 0.3536 0.1626	0.4407 0.239 0.5996	0.1961 0.156	0.4366
	L1	C1	L2	C2	L3	C3	L4 ,	C4	L6	C6
	Ø		·@= [•		0	un un	(ch)	1	

ble 11. Standardized component values for passive low-pass filters with an input impedance to output impedance ratio 2:1 for even order sections and 1:1 for odd-order filters.

Tebb	12	Q	ام آ	•		0	*65			
n	L1	C1	12	C2	L3	C3	L4	C4	L5	C5
2	0.2214	0.1304							-	
3	0.2408	0.2402	0.114					1	1	
4	0.2404	0.2814	0.2316	0.107				1		
5	0.2465	0.2876	0.2811	0.2255	0.1036					
6	0.2441	0.2998	0.2913	0.2763	0.2218	0.1016		1	1	
7	0.2506	0.2957	0.3057	0.2908	0.275	0.2914	0.1004		1	
8	0.2454	0.3041	0.3025	0.3084	0.2897	0.2742	0.2178	0.0996	i	
9	0.2515	0.298	0.3117	0.3039	0.305	0.2885	0.273	0.2166	0.09904	
10	0.2461	0.3058	0.3058	0.3135	0.304	0.3055	0.2876	0.272	0.2158	0.08854

Table 12. Standardized component values for passive low-pass sections with negligible source impedance.

0.2137 0.5466 0.2621 0.344 0 2788 10 0.03947 0.8834 0.1145 0.8982 0.1764

'n	C1	C2	C1	C2	C3
2	0.2607	0.1107			1
3			1,0589	0.2905	0.02141
4	0.7308 0.3024	0.03836 0.1975			
5	1,0838	0.02515	0.7078	0.4011	0.06054
8	1,5169 0.555 0.4063	0.01767 0.07826 0.2827			
7	2,026 0.7235	0.01304 0.05301	0 8236	0.6287	0.09081
8	2,8165 0.8188 0.8138 0.3813	0.01001 0.03817 0.1097 0.3697			Ì
8	3,265 1,1411 0.7445	0.00793 0.02884 0.07408	0.9656	0.5822	0.1191
10	4,0298 1,3869 0.8917 0.7078 0.6384	0.00643 0.02258 0.0534 0.1394 0.4679			

Table 13. Standardized component values for active filters with single feedback path.



Tables 10-14 give all information necessary for the computation of Chebishev filters from the 2nd to the 10th order with a ripple of 0.1 dB. Note, however, that the values for odd-order filters in Table 11 apply to sections whose input to output impedance ratio is 1:2 (if a T configuration) or 2: (if a x filter).

The gain vs frequency curves in Fig. 42 clearly show the sharp profile of this type of filter, while the ripple is hardly noticeable. The delay time vs frequency curves in Fig. 43 give a rather worse picture than those of the filter discussed in previous parts of this article. The step response in Fig. 44 clearly shows the ringing. Note that the curves in Fig. 43 and Fig. 44 do not improve all that much if a lower value ripple is chosen.

Two examples

As in previous parts, we give two examples of how to compute a filter. This time, we take a band-pass filter and a complex low-pass section in a double opamp configuration.

Example 1.

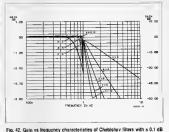
Compute a passive band-pass filter with a centre frequency of 1 kHz and a bandwidth of 100 Hz. The attenuation at 900 Hz and 1100 Hz must be at least 20 dB. The output impedance is to be $600~\Omega$ and the output impedance of the amplifier to which the filter is to be connected is negligible.

Solution.

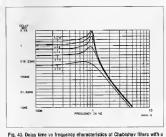
Since the centre frequency is known, it need not be computed. We calculate the frequencies corresponding to 900 Hz and 1100 Hz but at the opposite side of the filter referred to the centre frequency to find the sharpest roll-off. The frequency associated with 900 Hz is:

$$f_2 = 1000^2 / 900 = 1111 \text{ Hz}.$$

and that associated with 1100 Hz is:



ripple.



0.1 dB rippie.

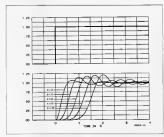


Fig. 44. Step response of Chebishev filters with a 0.1 dB ripple.

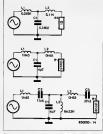


Fig. 45. Designing a passive band-pass filter: (a) standardized high-pass section; adjusting values for required bandwidth; (c) conversion to band-pass filter

$$f_1{=}\,1000^2\,/\,1100 = 909$$
 Hz.

The frequencies closest to 1 kHz are 909 Hz and 1100 Hz, so that the bandwidth at the -20 dB points is 191 Hz.

In the characteristics, we now have to find a filter that provides an attenuation of not less than 20 dB at a standardized frequency of 19/100 = 19 Hz (note that for a low-pass section the bandwidth, not the central frequency, is the basis of the design). From the data, we choose a third-order, 0.1 dB Chebishev section: this provides an attenuation of about 22 dB at f=2 Hz (estimated between a second- and a fourth-order filter).

Figure 45a shows the circuit diagram of a third-order low-pass section. The standardized component values are derived from Table 12. Next, the 'real' values are calculated for a terminal impedance of 600 Ω and a cut-off frequency equal to the -3 dB bandwidth (100 Hz).

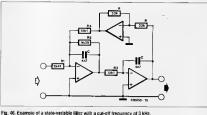
$$L_1 = LR/f = 1.4448 \text{ H}$$

$$C_1 = C/Rf = 4.003 \times 10^{-6} = 4 \mu F$$

$$L_2 = LR/f = 0.684 \text{ H}$$

Then follows the transformation from a low-pass to a band-pass filter as explained in Part 5, which results in the filter shown in Fig. 45c. The remaining components are calculated with the aid of formulas [34] and [35] (Part 5):

$$C_2 = 1/L(2\pi f_c)^2 = 1/1.45(2\pi 1000)^2 =$$



g. 40. Example of a state-variable filler with a cur-on frequency of 3 kmz.

$$L_3 = 1/C_1(2\pi f_C)^2 = 1/4 \times 10^{-6}(2\pi 1000)^2 =$$

$$= 6.33 \times 10^{-3} = 6.33 \text{ mH}$$

$$C_3 = 1/L_2(2\pi f_C)^2 = 1/0.68(2\pi 1000)^2 =$$

= 3.73×10⁻⁸ = 37.3 nF

Note that the central frequency of the band-pass section is used only for the computation of the values of those components that are added during the conversion process.

Example 2,

Design an active high-pass filter with a cut-off frequency of 3 kHz and a slope of 12 dB/octave. It is essential that the cut-off frequency can be set accurately. The gain of the section must be 14 dB (×5).

Solution

This type of section is best realized by a state-variable filter (see Fig. 17 – Part 3). For convenience, we again choose a Chebishev filter. The state-variable filter is based on the poles of a second-order filter in Table 10:

 $-\alpha = 0.6074$

$$\beta = \pm 0.7112$$

First, we choose a value for C, say, 4.7 nF. Resistors R are given a value of 33 k Ω . The other resistor values are then calculated with the aid of formulas [19], [20], [21] and [22], but note that all values so obtained must be divided by the cut-off frequency since the formulas give values for f = 1 Hz.

 $R_1 = 1/[2\pi f_k A C \sqrt{(\alpha^2 + \beta^2)}] =$ = $1/2\pi \times 3000 \times 5 \times 4.7 \times 10^{-9} \times$ $\times \sqrt{(0.6074^2 + 0.7112^2)} = 2414 \Omega$

$$R_2 = 1/4\pi\alpha C f_k =$$

= $1/4\pi \times 3000 \times 0.6074 \times 4.7 \times 10^{-9} =$
= 9291Ω

$$R_3 = R_4 = 1/2\pi C f_k \sqrt{(\alpha^2 + \beta^2)} =$$

= 1/2\pi \text{3000}\times 4.7\times 10^{-9}\times
\times (0.6074^2 + 0.7112^2) = 12068 \Omega

Resistors R₂ and R₄ may be a combination of a fixed resistor and a preset potentiometer to enable the cut-off frequency and Q-factor of the section to be set accurately.

Correction to Part 3

From the foregoing in this part of the series, you will have noticed that resistors R_2 and R_4 and R_5 (as stated in Part 3) are used for setting the parameters of the state-variable section. Thus, R_5 serves to set the maximum output voltage of A_1 at f_0 , while R_2 is used to set the bandwidth to the value at which the Q-factor is calculated.

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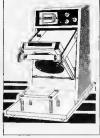
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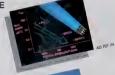
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